

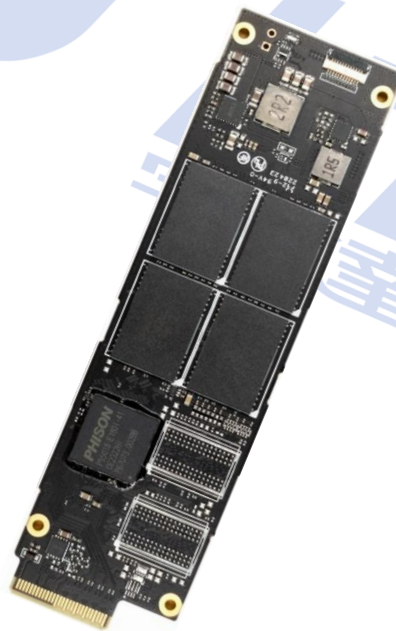
UD info Corp.

Industrial EDSFF E1.S PCIe SSD

FIPS 140-3

E1S-56DB Series

Product DataSheet



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3F-4, No.8, Ln. 609, Sec. 5, Chongxin Rd., Sanchong Dist., New Taipei City 241, Taiwan (R.O.C.)

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Revision History

Revision	Draft Date	History	Author
Preliminary	2025/9/24	Preliminary version	Golden Lee



Product Overview

- **Capacity**
 - 1TB up to 8TB
 - * 8TB only support in C-temp
- **Form Factor**
 - EDSFF E1.S (9.5mm)
- **PCIe Interface**
 - PCIe Gen4 x4
 - NVMe 1.4
 - PCI Express Base 4.0
- **Performance¹**
 - Sequential Read up to 7,000 MB/s
 - Sequential Write up to 2,000 MB/s
 - Random 4k Read up to 850K IOPS
 - Random 4K Write up to 500K IOPS
- **Temperature Range²**
 - Operation Temperature:
 - Standard: 0°C ~ 70°C
 - Wide: -40°C ~ 85°C
 - Storage Temperature:
 - -40°C ~ 85°C
- **Power Consumption³**
 - Active mode (Max.): < 12W
 - Idle mode: < 3.1W
- **ECC**
 - LDPC / RAID ECC
 - Low density parity check code
(>120buit/KBytes)
- **Reliability**
 - MTBF: 2 million hours
 - UBER: < 1 sector per 10¹⁶ bits
 - TBW: TBC
 - DWPD ≥ TBC
- **Environment Specification**
 - Shock: 1500G_{0-P}/0.5ms duration
 - Vibration: 20Hz~80Hz/1.52mm
80Hz~2000Hz/20G_{P-P}
 - Drop: 80cm height/each face
 - Conflicting Material: Concrete floor
- **RoHS Compliant**
- **EMI Compliant**
 - CE: EN55032, CISPR 32
 - FCC: ANSI C63.4
 - BSMI: CNS 15936
 - VCCI: CISPR 32
- **Features Support List**
 - TCG Pyrite/OPAL
 - FIPS 140-3 Iv2 **on going:**
Certificate number #

Notes:

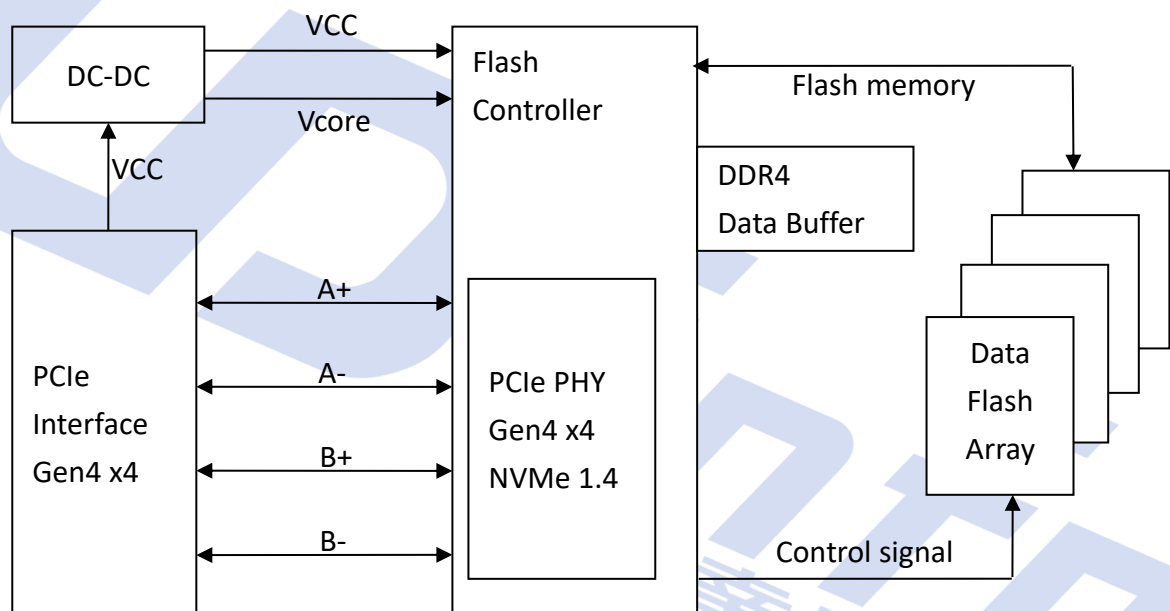
1. Refer to Chapter 2.3 for more details.
2. The operation temperature means the case temperature, in which can be detected via the S.M.A.R.T.
Operation temperature range depends on NAND flash applied capability, which maximum value is listed.
3. Refer to Chapter 4, section 4.2 power consumption for more details.

1. INTRODUCTION

1.1. General Description

This document describes the specifications of UDinfo E1.S PCIe Solid State Drive. UDinfo E1.S delivers all the advantages of flash disk technology with PCIe Gen4x4 interface. It offers a wide range capacity up to 8TB and its performance can reach up to 7,000 MB/s (for read) and 2,000 MB/s (for write) based on 112Layers 3D TLC NAND flash with the choice of 1GB/2GB/4GB DDR4.

1.2. Block Diagram



E1.S PCIe SSD Block Diagram

2. PRODUCT SPECIFICATIONS



2.1. Product Specifications

- **Capacity**
 - 1TB up to 8TB⁴
- **Electrical/Physical Interface**
 - PCIe Interface
 - PCI Express Base Ver 4.0
 - Compliant with NVMe 1.4
 - PCIe Gen4 x 4 lane & backward compatible to PCIe Gen3, Gen2 and Gen1

2.2. Device Capacity

Capacity	IDEMA Standard		User Data Size
	512Bytes/Sector	4KBytes/Sector	
	Total Sectors (LBA)	Total Sectors (LBA)	
1TB	2,000,409,264	250,051,158	Depended on file management
2TB	4,000,797,360	500,099,670	
4TB	8,001,573,552	1,000,196,694	
8TB ⁴	16,003,125,936	2,000,390,742	

Notes:

1. 1 Gigabyte (GB) is equal to 1,000,000,000 Bytes; 1 sector is equal to 512 Bytes or 4K Bytes.
2. The calculation is following IDEMA Standard.
3. The total actual user data size of the SSD may be less than device capacity due to SSD format, SSD partition, operating system.
EX: OS shows 953.87GB (NTFS) on 1TB device.
4. 8TB only support in c-temp

2.3. Performance

Capacity	Flash Structure	Sequential (MB/s)		Random (IOPS)	
		Read	Write	Read	Write
1TB	Kioxia BiCS5, 512Gb 112Layers	6,800	700	270K	180K
2TB	Kioxia BiCS5, 512Gb 112Layers	7,000	1,400	500K	350K
4TB	Kioxia BiCS5, 512Gb 112Layers	4,800	2,000	500K	500K
8TB	Kioxia BiCS5, 1Tb 112Layers	6,600	1,800	850K	440K

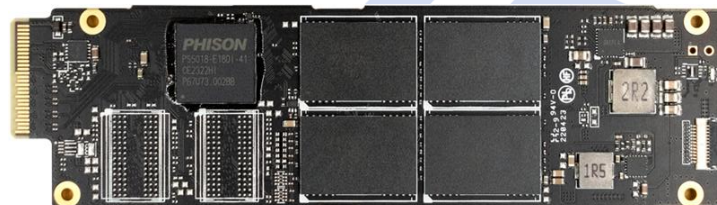
Notes:

1. Adopts dynamic caching to deliver better performance and consumer user experience.
2. Performance may differ according to flash configuration, use condition, environment and platform.
3. Performance specification is under Thermal Throttling inactivated.
4. Tested with CrystalDiskMark 8.0, QD8T1, 1GB range for Sequential performance.
5. Tested with IOMeter, 1GB range, 4K data size, QD=128, 16 worker, 4k aligned for Random IOPS.
6. Operating System: Windows 10 Professional (x64); Intel Core i7-8700K CPU @ 3.70GHz
7. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+12V condition.

2.4. Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. The E1S-56DH is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via S.M.A.R.T. reading.

- **Purpose of Thermal Throttling:**
 - In order to keep the optimal performance in the safe range of the temperature.
- **Thermal sensors:**
 - We have external thermal sensor & on-die thermal sensor (internal controller) to detect temperature. There is 1pcs external thermal sensor on PCB, the position depends on different form factor (The thermal sensor is shown below. The picture is for reference only).
 - External thermal sensor would detect flash temperature; On-die thermal sensor detect controller temperature.



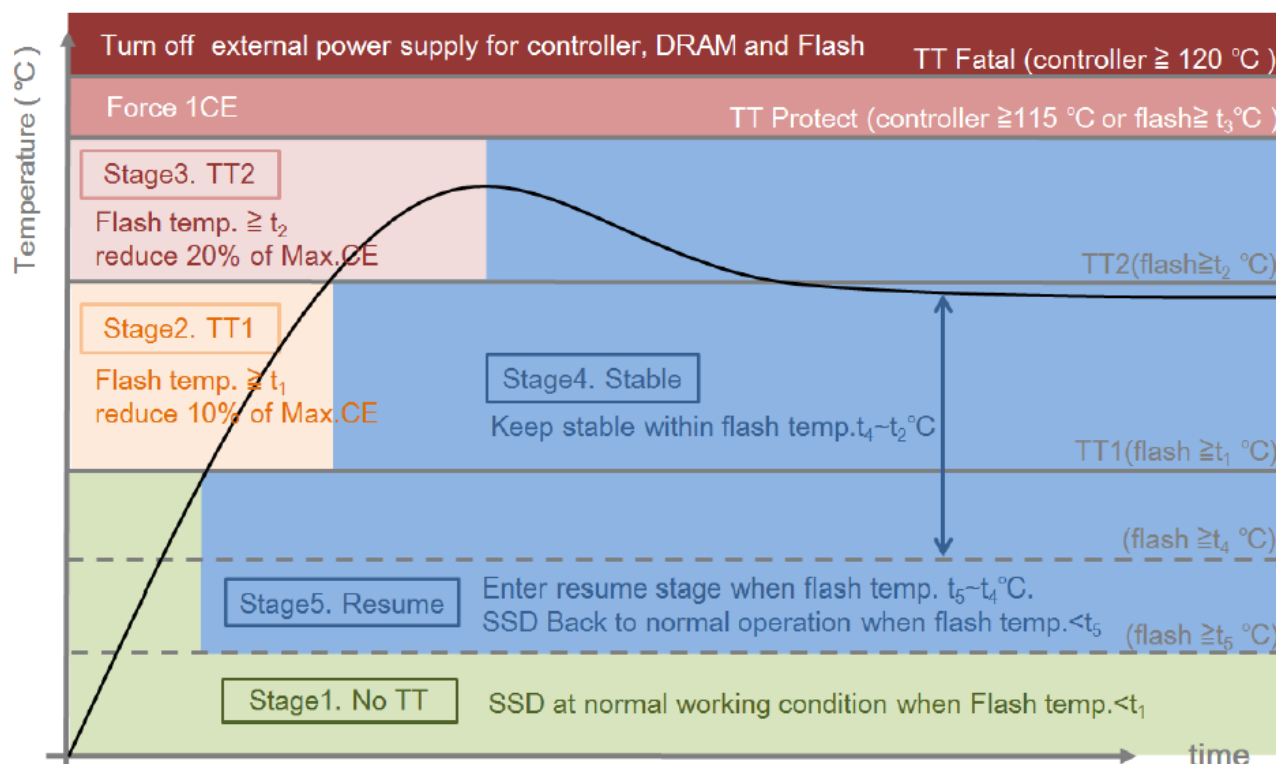


Figure 2-1 Thermal Throttling Schematic

	Operation temp. of Normal-temp. grade: 0°C ~ 70°C	Operation temp. of Wide-temp. grade: -40°C ~ 85°C
t₁	76°C	82°C
t₂	78°C	85°C
t₃	88°C	95°C
t₄	72°C	78°C
t₅	68°C	74°C

Notes:

1. TT shown on Figure 2-1 means "Thermal Throttling".
2. CE = Chip Enable.
3. temp. = temperature

2.5. TCG Opal 2.0 (Optional)

The Opal specification is a set of specifications for self-encrypting drives published by the Trusted Computing Group (TCG), a non-profit organization that develops, defines, and promotes standards and specifications for secure computing. The Opal Security Subsystem Class(SSC) 2.0 defines the details of data management in storage devices and the classes authority for data access, and secures data from theft and tampering by unauthorized persons who are able to gain access to the storage device or host system.

TCG Opal 2.0 Main Features:

- AES 256-bit Hardware Self Encryption
- Deploy Storage Device & Take Ownership:
The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- Activate or Enroll Storage Device:
LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- Lock & Unlock Storage Device:
Unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- Repurpose & End-of-Life:
Erasure of data within one or more.
- Physical Presence SID (PSID):
PSID is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

3. ENVIRONMENTAL SPECIFICATIONS



3.1. Environmental Conditions

3.1.1. Temperature Specification

	Mode	Min.	Max.	Unit
Temperature Ranges	Operation (Standard)	0	70	°C
	Operation (Wide)	-40	85	°C
	Storage	-40	85	°C
Humidity	Operation	5	95	%
	Storage	5	95	%
Temperature Cycle Test	Operation (Standard)	0	70	°C
	Operation (Wide)	-40	85	°C
	Storage	-40	85	°C

Notes:

1. The operation temperature means the case temperature, in which can be detected via the S.M.A.R.T. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.

3.1.2. Mechanical Specification

Items			Condition
Shock	Non-operational	Acceleration Force	1500G 0-p with half sine wave (0.5ms)
Vibration	Non-operational	Frequency/Displacement	20Hz~80Hz/1.52mm
		Frequency/Acceleration	80Hz~2000Hz/20G p-p with sine wave
Drop	Non-operational	Height of Drop	80cm free fall
		Number of Drop	6 face of each unit
		Conflicting Material	Concrete floor

3.1.3. Electrostatic Discharge (ESD)

Specification	+/- 4KV
EN 55035, CISPR 35 EN 61000-4-2 and IEC 61000-4-2	Device functions are affected, but EUT will be back to its normal or operational state automatically.

3.1.4. EMI Compliance

Specification
CE: EN 55032, CISPR 32
FCC: ANSI C63.4
VCCI: CISPR 32
BSMI: CNS 15936

3.2. TBW (TeraBytes Written) and DDPD (Drive Write Per Day)

Capacity	Flash Type	TBW	DDPD
1TB	Kioxia BiCS5, 512Gb 112Layers	TBC	TBC
2TB	Kioxia BiCS5, 512Gb 112Layers	TBC	TBC
4TB	Kioxia BiCS5, 512Gb 112Layers	TBC	TBC
8TB	Kioxia BiCS5, 1Tb 112Layers	TBC	TBC

Notes:

- TBW is measured by JEDEC Client 219A workload.
(a) TLC: Calculated with PE count = 3000.
- TBW may differ according to flash configuration and platform.
- DDPD is calculated based on 3-year lifetime.
- $DDPD = TBW / (365 \times 3\text{years} \times \text{User capacity})$
- The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected. (Like certain Windows OS, Linux kernel version before 2.6.33, other OS please reference each own user manual)
- The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.

3.3. UBER

Capacity	UBER
1TB ~ 8TB	< 1 sector per 10^{16} bits read

Notes:

1. UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.
2. $UBER = FER \text{ (fail rate)} / \text{Data Size (user data bit)}$.
3. $FER = \text{uncorrectable ECC frame number} / \text{total ECC frame number}$.
4. The LDPC for TLC ECC capability > 120bit/KB.

3.4. MTBF

MTBF, Mean Time between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex 7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

Capacity	MTBF
1TB ~ 8TB	2 million hours

4. ELECTRICAL SPECIFICATIONS



4.1. Supply Voltage

Parameter	Rating
Operating Voltage	12V $\pm$ 5%
Rise Time (Max/Min)	100ms / 0.1ms
Fall Time (Max/Min)	5s / 10ms
Min. off Time ^{Note1}	1s

Notes:

1. Minimum time between power removed from SSD ($V_{cc} < 100$ mV) and power re-applied to the drive.
2. Ensure the voltage of each power domain in SSD has enough time to discharge less than 0.1V.
3. Rise Time during from 10% to 90% of 12V.
4. Fall Time during from 90% to 10% of 12V.

4.2. Power Consumption

Capacity	Flash Structure	Read	Write	Idle
1TB	Kioxia BiCS5, 512Gb 112Layers	9	8	3.1
2TB	Kioxia BiCS5, 512Gb 112Layers	10	8	3.1
4TB	Kioxia BiCS5, 512Gb 112Layers	11	11	3.1
8TB	Kioxia BiCS5, 1Tb 112Layers	11.7	11.8	3.1

Unit: W

Notes:

1. Use CrystalDiskMark 7.0.0 with the setting of 1GB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5].
2. Power consumption may differ according to flash configuration, use condition, environment and platform.
3. The measured power voltage is 12V.
4. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+12V condition.

5. INTERFACE



5.1. Pin Assignment and Descriptions

The table 5-1 defines the signal assignment of the internal EDSFF connector for SSD usage, described in the PUBLISHED_SFF-TA-1009_R3.1 of PCIE SIG.

Table 5-1 Pin Assignment and Description of EDSFF E1.S

Pin #	PCIe Pin	Description
A1	GND	Return current path
A2	GND	Return current path
A3	GND	Return current path
A4	GND	Return current path
A5	GND	Return current path
A6	GND	Return current path
A7	SMBCLK	SMBCLK: Open Drain with pull-up on host. SMBus Clock.
A8	SMBDATA	SMBDATA: Open Drain with pull-up on host. SMBus Data.
A9	SMRST#	Active low signal. SMRST# is a reset for the management interface.
A10	LED	Active high signal. This signal is used to drive the amber or amber/blue LED state from the host to the device.
A11	CLKREQ#	CLKREQ#: Clock Request is a reference clock request signal defined by the PCI Express Base Specification. It may be supported by a device in single port mode only. If CLKREQ# is supported by the host and the device, then the signal is Open Drain with a pull up on host.
A12	PRSNT0#	Active low signal. This signal indicates to the host that the device is electrically attached.
A13	GND	Return current path
A14	REFCLKn1	NC
A15	REFCLKp1	NC
A16	GND	Return current path
A17	PERn0	PCIe RX Differential signals defined by the PCI Express Card Electromechanical Specification.
A18	PERp0	PCIe RX Differential signals defined by the PCI Express Card Electromechanical Specification.
A19	GND	Return current path
A20	PERn1	PCIe RX Differential signals defined by the PCI Express Card Electromechanical Specification.

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Pin #	PCle Pin	Description
A21	PERp1	PCle RX Differential signals defined by the PCI Express Card Electromechanical Specification.
A22	GND	Return current path
A23	PERn2	PCle RX Differential signals defined by the PCI Express Card Electromechanical Specification.
A24	PERp2	PCle RX Differential signals defined by the PCI Express Card Electromechanical Specification.
A25	GND	Return current path
A26	PERn3	PCle RX Differential signals defined by the PCI Express Card Electromechanical Specification.
A27	PERp3	PCle RX Differential signals defined by the PCI Express Card Electromechanical Specification.
A28	GND	Return current path
B1	12V	12V Power
B2	12V	12V Power
B3	12V	12V Power
B4	12V	12V Power
B5	12V	12V Power
B6	12V	12V Power
B7	MFG	NC
B8	PFU	NC
B9	DUALPORTEN#	NC
B10	PERST0#	PE-Reset is a fundamental reset to the device defined as PERST# by the PCI Express Base Specification.
B11	3.3 Vaux	3.3V Power
B12	PWRDIS	Active high signal. Power Disable notifies the device to turn off all systems connected to 12V power.
B13	GND	Return current path
B14	REFCLKn0	PCle Reference Clock signals defined by the PCI Express Base Specification.
B15	REFCLKp0	PCle Reference Clock signals defined by the PCI Express Base Specification.
B16	GND	Return current path
B17	PETn0	PCle TX Differential signals defined by the PCI Express Card Electromechanical Specification.
B18	PETp0	PCle TX Differential signals defined by the PCI Express Card Electromechanical Specification.
B19	GND	Return current path

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Pin #	PCIe Pin	Description
B20	PETn1	PCIe TX Differential signals defined by the PCI Express Card Electromechanical Specification.
B21	PETp1	PCIe TX Differential signals defined by the PCI Express Card Electromechanical Specification.
B22	GND	Return current path
B23	PETn2	PCIe TX Differential signals defined by the PCI Express Card Electromechanical Specification.
B24	PETp2	PCIe TX Differential signals defined by the PCI Express Card Electromechanical Specification.
B25	GND	Return current path
B26	PETn3	PCIe TX Differential signals defined by the PCI Express Card Electromechanical Specification.
B27	PETp3	PCIe TX Differential signals defined by the PCI Express Card Electromechanical Specification.
B28	GND	Return current path

6. SUPPORTED COMMANDS



6.1. NVMe Command List

Table 6-1 Admin Commands

Identifier	O/M	Command Description
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Features
0Ah	M	Get Features
0Ch	M	Asynchronous Event Request
10h	O	Firmware Activate
11h	O	Firmware Image Download
14h	O	Device Self-test
80h	O	Format NVM
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize

Table 6-2 I/O Commands

Identifier	O/M	Command Description
00h	M	Flush
01h	M	Write
02h	M	Read
04h	O	Write Uncorrectable
05h	O	Compare
08h	O	Write Zeroes
09h	O	Dataset Management

Table 6-3 Set Feature Commands

Identifier	O/M	Command Description
00h		Reserved
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Dh	O	Host Memory Buffer
0Eh	O	Timestamp
10h	O	Host Controlled Thermal Management
11h	O	Non-Operational Power State Config
0Eh – 7Dh		Reserved
80h	O	Software Progress Marker

Table 6-4 Get Log Page Commands

Identifier	O/M	Command Description
00h		Reserved
01h	M	Error Information
02h	M	SMART / Health Information
03h	M	Firmware Slot Information
04h	O	Changed Namespace List
06h	O	Device Self-test
09h - 7Fh		Reserved
81h	O	Sanitize Status
82h - FFh		Reserved

6.2. Identify Device Command

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-5 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	TBD
63:24	M	Model Number (MN)	TBD
71:64	M	Firmware Revision (FR)	TBD
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	0x6479A7
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0001
83:80	M	Version (VER)	0x00010300
87:84	M	RTD3 Resume Latency (RTD3R)	0x00989680
91:88	M	RTD3 Entry Latency (RTD3E)	0x00989680
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000200
99:96	M	Controller Attributes (CTRATT)	0x0002
111:100	O	Reserved	0x00
127:112	O	FRU Globally Unique Identifier (FGUID)	0x00
239:128	-	Reserved	0x00
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x0387010000000000 0000000000000000
257:256	M	Optional Admin Command Support (OACS)	0x0017
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x08
262	M	Error Log Page Entries (ELPE)	0x3E
263	M	Number of Power States Support (NPSS)	0x00
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x00

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Bytes	O/M	Description	Default Value
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x015C
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0161
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0064
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000
295:280	O	Total NVM Capacity (TNVMCAP)	**
311:296	O	Unallocated NVM Capacity (UNVMCAP)	**
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00000000
317:316	O	Extended Device Self-test Time (EDSTT)	0x000A
318	O	Device Self-test Options (DSTO)	0x00
319	M	Firmware Update Granularity (FWUG)	0x01
321:320	M	Keep Alive Support (KAS)	0x0000
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x0001
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x0139
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x0166
331:328	O	Sanitize Capabilities (SANICAP)	0x07
511:332	-	Reserved	0x00
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x0100
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0x005D
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x00
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	TBD
529:528	M	Atomic Write Unit Power Fail (AWUPF)	TBD
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
767:540	M	Reserved	0x00
IO Command Set Attributes			

Bytes	O/M	Description	Default Value
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	0x00
1791:1024	-	Reserved	0x00
2047:1792	-	Reserved	0x00
2079:2048	M	Power State 0 Descriptor (PSD0)	TBD
2111:2080	O	Power State 1 Descriptor (PSD1)	0x00
2143:2112	O	Power State 2 Descriptor (PSD2)	0x00
2175:2144	O	Power State 3 Descriptor (PSD3)	0x00
2207:2176	O	Power State 4 Descriptor (PSD4)	0x00
2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00

Bytes	O/M	Description	Default Value
Vendor Specific			
3278:3072	O	Vendor Specific (VS)	0x00
3279	O	Vendor Specific (VS)	0x00
4095:3080	O	Vendor Specific (VS)	Vendor Reserved

* The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at

<http://standards.ieee.org/develop/regauth/oui/public.html>.

** Depends on the using of capacity



Table 6-6 Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	TBD*
15:8	M	Namespace Capacity (NCAP)	TBD*
23:16	M	Namespace Utilization (NUSE)	TBD*
24	M	Namespace Features (NSFEAT)	0x00
25	M	Number of LBA Formats (NLBAF)	0x01
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x00
28	M	End-to-end Data Protection Capabilities (DPC)	0x00
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x00
31	O	Reservation Capabilities (RESCAP)	0x00
32	O	Format Progress Indicator (FPI)	0x00
33		Reserved	0x09
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46		Reserved	0x0000
63:48	O	NVM Capacity (NVMCAP)	0x00
103:64		Reserved	0x00
119:104	O	Namespace Globally Unique Identifier (NGUID)	0x00
127:120	O	IEEE Extended Unique Identifier (EUI64)	0x373900F0FFA77964
131:128	M	LBA Format 0 Support (LBAF0)	0x02090000
135:132	O	LBA Format 1 Support (LBAF1)	0x00000000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000

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Bytes	O/M	Description	Default Value
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000
383:192		Reserved	0x00

* See IDEMA SPEC

** See IEEE EUI-64 SPEC

“O/M”: O = Optional, M = Mandatory.

“-”: Not support

■ List of Identify Namespace Data Structure for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)
1,024	773BD2B0h
2,048	EE7752B0h
4,096	1DCEE52B0h
8,192	3B9DC52B0h

6.3. SMART Attributes

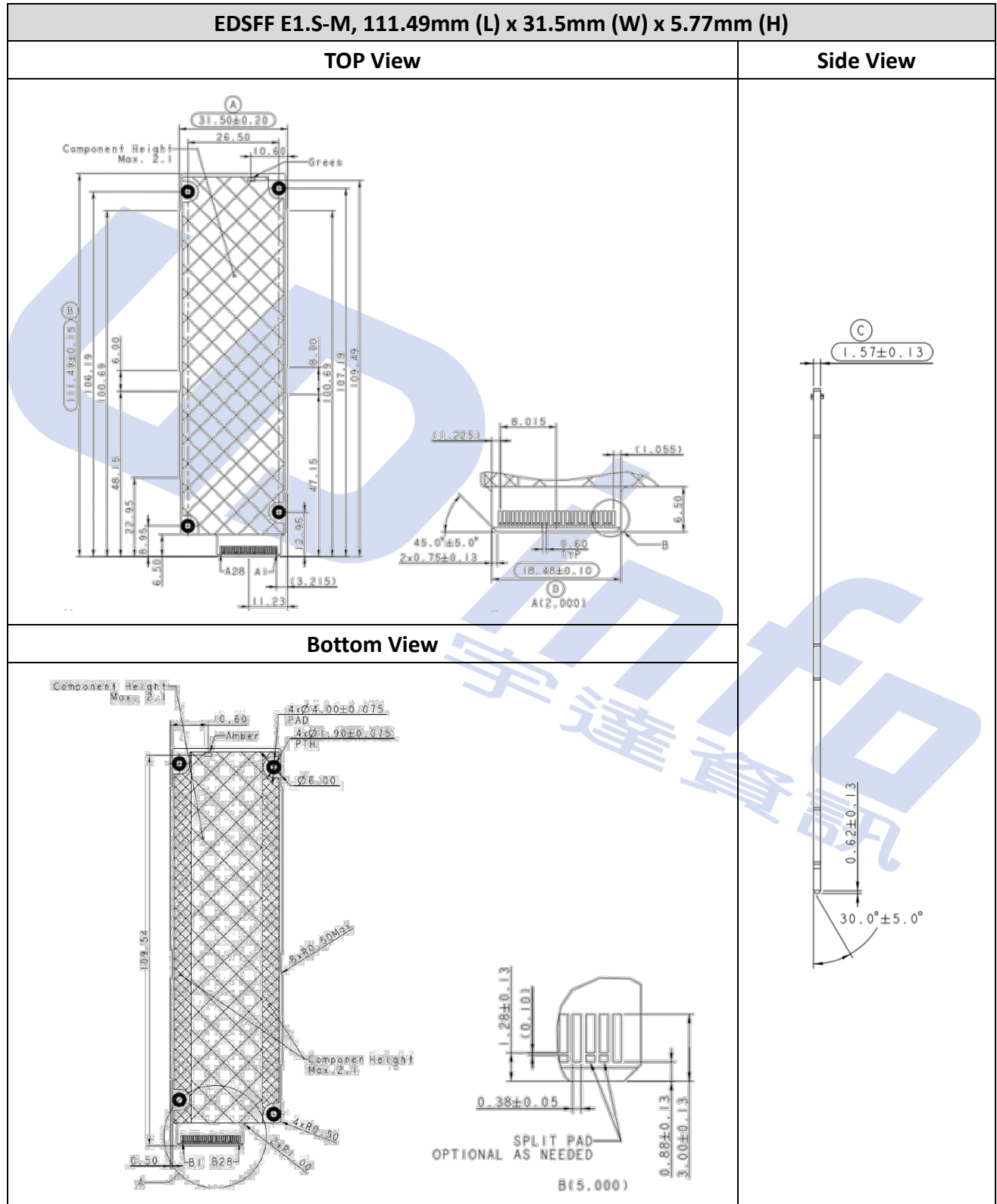
■ SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (CTRL Tj)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved

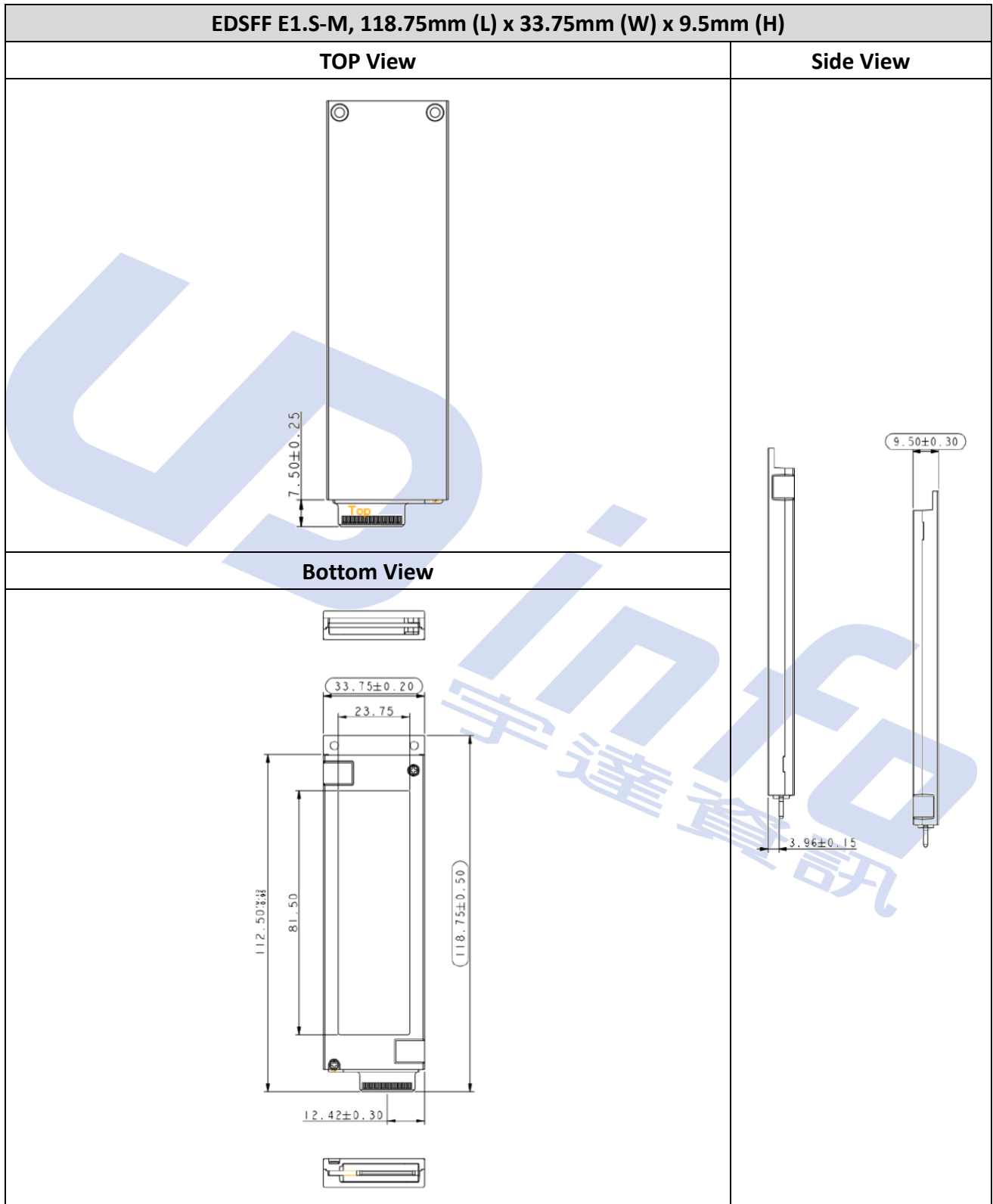
7. PHYSICAL DIMENSION



7.1. EDSFF E1.S Mechanical Diagram



7.2. EDSFF E1.S 9.5mm Mechanical Diagram



8. ORDERING INFORMATION



Capacity	Part Number
1TB	E1S-56DB001TB-BFP
2TB	E1S-56DB002TB-BFP
4TB	E1S-56DB004TB-BFP
8TB	E1S-56DB008TB-AFP



9. REFERENCE



The following table is to list out the standards that have been adopted for designing the product.

Table 9-1 List of References

Title	Source
PCI Express® Base Specification Rev. 4.0	https://www.pcisig.com/specifications/pciexpress/base3/
NVM Express® Base Specification Rev. 1.4	http://www.nvmexpress.org/
SFF-TA-1009	https://members.snia.org/document/dl/26728
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a