Product Datasheet

UD info Corp.

PCMCIA ATA Flash Card

Product Specification

Version 1.2

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Contents:

1. Scope

This document describes the features and specifications and installation guide of AFAYA's *PCMCIA-ATA FLASH CARD* Products.

2. Introduction

The *PCMCIA-ATA FLASH CARD* is solid-state design and IDE compatible.
It is an ideal replacement for standard IDE hard disks.
It's a solid-state design offers no seek errors even under extreme shock and vibration conditions. The *PCMCIA-ATA FLASH CARD* is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The *PCMCIA-ATA FLASH CARD* is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The *PCMCIA-ATA FLASH CARD* is IDE compatible and offering various capacities. It has low power consumption and can operate from a single 3.3/5.0 Volt power supply. The *PCMCIA-ATA FLASH CARD* provides memory storage for mobile computing applications, consumer electronics and embedded systems. It is fully compatible with existing systems.

3. System Features

- Operating Modes:
  - PC Card Memory Mode.
  - PC Card I/O Mode.
  - True-IDE Mode.
- Host Interface Supports
  - Multi-Word DMA Modes 0~4
  - Ultra DMA Modes 0~6
  - PCMCIA Extended Memory Mode Cycle time: 250, 120, 100, 80ns
  - PCMCIA Ultra DMA Modes 0~6
- Hardware RS-code ECC capable of correcting 24 bits in a 1,024 byte data
- Reliable Wear-leveling algorithm to ensure the best of flash endurance.
- Very low power consumption
- Very high performance
- Rugged environment is working well
- Automatic error correction and retry capabilities
- Supports power down commands and Auto Stand-by / Sleep Mode
- +5 V ±10% or +3.3 V ±5% operation
- MTBF > 2,000,000 hours
- Capacity: 128MB, 256MB, 512 MB, 1GB, 2GB, 4GB, 8GB, 16GB, 32GB(unformatted)

4. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

4.1. System Environmental Specification

Referral Part Number		ATA68SIXXXX[1]BX[2]X[3]X[4]
Standard Temperature	Operating	0ºC ~ +70ºC
	Non-operating	-20ºC ~ +80ºC
Wide Temperature	Operating	-40ºC ~ +85ºC
	Non-operating	-50ºC ~ +95ºC
Humidity	Operating	5% ~ 95% non-condensing
	Non-operating	
Vibration	Operating	15G peak-to-peak maximum
	Non-operating	
Shock	Operating	2000 G maximum
	Non-operating	
Altitude	Operating	50,000 feet maximum
	Non-operating	

Note:

1) *XXXX[1]: Capacity, include 128MB ,256M, 512M, 001G, 002G, 004G, 008G ,016GB and 032G*
2) *X[2]:Temperature Grade I: (Wide temperature) C: (Standard temperature)*
3) *X[1]: Disk mode, include F:(Fixed Disk Mode) ,R: (Removable Disk Mode) and, A: Auto Detect Disk Mode*
4) *X[4]:Transfer mode, include P:(PIO mode) ,M:(Multi-Word Mode) and, U:(UDMA mode)*

4.2. System Power Requirement

Referral Part Number		ATA68SIXXXX[1]BX[2]X[3]X[4]
DC Input Voltage 100mV max. ripple (p-p)		5V±10%
+5V Current (Maximum average value)	Standby Mode:	12mA
	Reading Mode:	95mA
	Writing Mode:	140mA

Note:

1) *XXXX[1]: Capacity, include 128MB ,256M, 512M, 001G, 002G, 004G, 008G ,016GB and 032G*
2) *X[2]:Temperature Grade I: (Wide temperature) C: (Standard temperature)*
3) *X[1]: Disk mode, include F:(Fixed Disk Mode) ,R: (Removable Disk Mode) and, A: Auto Detect Disk Mode*
4) *X[4]:Transfer mode, include P:(PIO mode),M:(Multi-Word Mode) and, U:(UDMA mode)*

4.3. System Performance

SLC Performance	**Sequential Read**	43 M bytes / sec Max.
	Sequential Write	35 M bytes / sec Max.
MLC Performance	**Sequential Read**	35 M bytes / sec Max.
	Sequential Write	15.5 M bytes / sec Max.

4.4. System Reliability

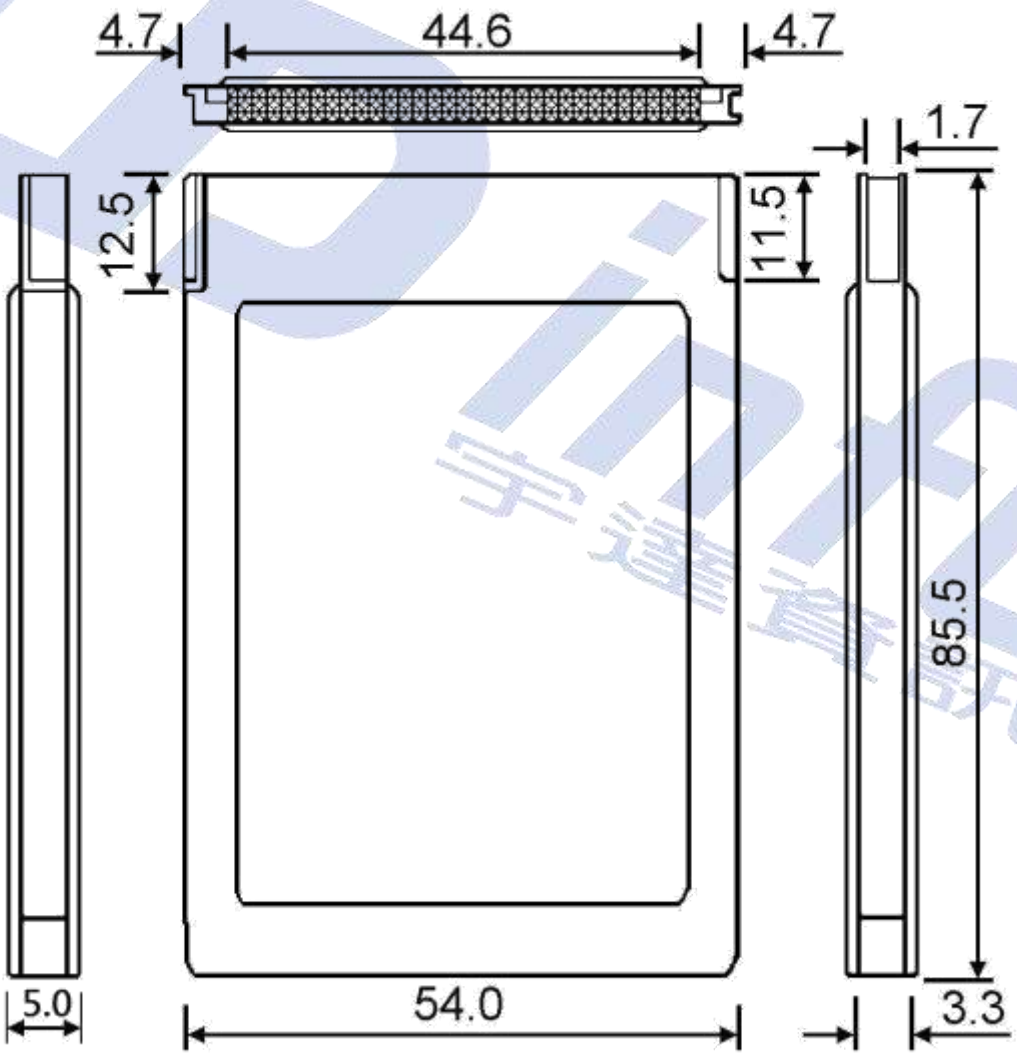
MTBF	> 2,000,000 hours
Data Reliability	< 1 non-recoverable error in 10^{14} bits read < 1 erroneous correction in 10^{20} bits read
Wear-leveling Algorithms	Supportive
ECC Technology	Hardware RS-code ECC capable of correcting 24 bits in a 1,024 byte data
Endurance (SLC)	Greater than 1,000,000 cycles Logically contributed by Wear-leveling and advanced bad sector management
Endurance (MLC)	Greater than 100,000 cycles Logically contributed by Wear-leveling and advanced bad sector management
Data Retention	10 years

4.5. Physical Characteristics

4.5.1. Physical Specifications

PCMCIA-ATA Flash Card	
Length:	85.5 ± 0.1 mm
Width:	54.4 ± 0.1 mm
Thickness:	5.0 ± 0.1 mm
Weight:	28.6 g (1.00 oz) maximum

4.5.2. PCMCIA-ATA Flash Card Dimension

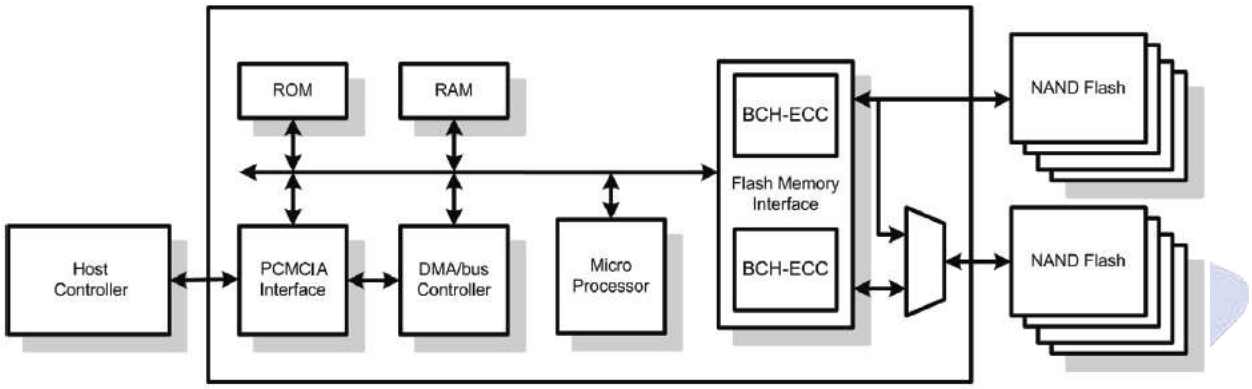


4.6. Capacity Specification

The specific capacities for the various models and the default number of heads, sectors and cylinders.

Capacity	Default Cylinder	Default Head	Default Sector	User Data Size
128MB	243	16	63	Depended on file management
256MB	487	16	63	
512MB	991	16	63	
1GB	1,966	16	63	
2GB	3,900	16	63	
4GB	7,785	16	63	
8GB	15,538	16	63	
16GB	31,045	16	63	
32GB	62,041	16	63	

4.7. Card Block Diagram



5. Interface Description

5.1. Pin Assignments

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type
1	GND	Ground	1	GND	Ground	1	GND	Ground
2	D3	I/O	2	D3	I/O	2	D3	I/O
3	D4	I/O	3	D4	I/O	3	D4	I/O
4	D5	I/O	4	D5	I/O	4	D5	I/O
5	D6	I/O	5	D6	I/O	5	D6	I/O
6	D7	I/O	6	D7	I/O	6	D7	I/O
7	CE1#	I	7	CE1#	I	7	CS0#	I
8	A10	I	8	A10	I	8	A10[2]	I
9	OE#	I	9	OE#	I	9	OE#	I
10	NC	-	10	NC	-	10	NC	-
11	A9	I	11	A9	I	11	A9[2]	I
12	A8	I	12	A8	I	12	A8[2]	I
13	NC	-	13	NC	-	13	NC	-
14	NC	-	14	NC	-	14	NC	-
15	WE#	I	15	WE#	I	15	WE#[3]	I
16	RDY/BSY#	O	16	IREQ#	O	16	INTRQ	O
17	VCC	Power	17	VCC	Power	17	VCC	Power
18	NC	-	18	NC	-	18	NC	-
19	NC	-	19	NC	-	19	NC	-
20	NC	-	20	NC	-	20	NC	-
21	NC	-	21	NC	-	21	NC	-
22	A7	I	22	A7	I	22	A7[2]	I
23	A6	I	23	A6	I	23	A6[2]	I
24	A5	I	24	A5	I	24	A5[2]	I
25	A4	I	25	A4	I	25	A4[2]	I
26	A3	I	26	A3	I	26	A3[2]	I
27	A2	I	27	A2	I	27	A2	I
28	A1	I	28	A1	I	28	A1	I
29	A0	I	29	A0	I	29	A0	I
30	D0	I/O	30	D0	I/O	30	D0	I/O
31	D1	I/O	31	D1	I/O	31	D1	I/O

32	D2	I/O	32	D2	I/O	32	D2	I/O
33	WP	O	33	IOIS16#	O	33	IOCS16#	O
34	GND	Ground	34	GND	Ground	34	GND	Ground
35	GND	Ground	35	GND	Ground	35	GND	Ground
Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type
36	CD1#	O	36	CD1#	O	36	CD1#	O
37	D11[1]	I/O	37	D11[1]	I/O	37	D11[1]	I/O
38	D12[1]	I/O	38	D12[1]	I/O	38	D12[1]	I/O
39	D13[1]	I/O	39	D13[1]	I/O	39	D13[1]	I/O
40	D14[1]	I/O	40	D14[1]	I/O	40	D14[1]	I/O
41	D15[1]	I/O	41	D15[1]	I/O	41	D15[1]	I/O
42	CE2#[1]	I	42	CE2#[1]	I	42	CS1#[1]	I
43	VS1#	O	43	VS1#	O	43	VS1#	O
44	IORD#	I	44	IORD#	I	44	IORD	I
45	IOWR#	I	45	IOWR#	I	45	IOWR	I
46	NC	-	46	NC	-	46	NC	-
47	NC	-	47	NC	-	47	NC	-
48	NC	-	48	NC	-	48	NC	-
49	NC	-	49	NC	-	49	NC	-
50	NC	-	50	NC	-	50	NC	-
51	VCC	Power	51	VCC	Power	51	VCC	Power
52	NC	-	52	NC	-	52	VPP	-
53	NC	-	53	NC	-	53	NC	-
54	NC	-	54	NC	-	54	NC	-
55	NC	-	55	NC	-	55	NC	-
56	NC	-	56	NC	-	56	CSEL#	-
57	VS2#	O	57	VS2#	O	57	VS2#	O
58	RESET	I	58	RESET	I	58	RESET#	I
59	WAIT#	O	59	WAIT#	O	59	IORDY	O
60	INPACK#	O	60	INPACK#	O	60	DREQ	O
61	REG#	I	61	REG#	I	61	DMACK	I
62	BVD2	I/O	62	SPKR#	I/O	62	DASP#	I/O
63	BVD1	I/O	63	STSCHG#	I/O	63	PDIAG#	I/O
64	D8[1]	I/O	64	D8[1]	I/O	64	D8[1]	I/O
65	D9[1]	I/O	65	D9[1]	I/O	65	D9[1]	I/O

66	D10[1]	I/O	66	D10[1]	I/O	66	D10[1]	I/O
67	CD2#	O	67	CD2#	O	67	CD2#	O
68	GND	Ground	68	GND	Ground	68	GND	Ground

Note:

1) 1. Signals marked with an asterisk are required for 16-bit access, not required when installed in 8-bit systems.

2) 2. Should be grounded by the host.

5.2. Pin Descriptions

Signal Name	Mode of predation	Pin Type	Pin No(s).	Description
CD1#, CD2#		O	36, 67	Card Detect Outputs
	PC Card Memory Mode			These Card Detect pins are connected to ground on the PC Card. They are used by the host to determine that the PC Card is fully inserted into the socket.
	PC Card I/O Mode			This signal is same in this mode.
	True IDE Mode			This signal is same in this mode.
IOWR#		I	45	I/O Write Input
	PC Card Memory Mode			This signal is not used in this mode.
	PC Card I/O Mode			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the PC Card controller registers. The clocking will occur on the negative to positive going edge of the signal.
	True IDE Mode			This signal has the same function as in PC Card I/O Mode.
IORD#		I	44	I/O Read Input
	PC Card Memory Mode			This signal is not used in this mode.
	PC Card I/O Mode			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the PC Card.
	True IDE Mode			This signal has the same function as in PC Card I/O Mode.
WE#		I	15	Write Enable Input

	PC Card Memory Mode			This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card. It is also used for writing the configuration registers.
	PC Card I/O Mode			In this mode, this signal is used to write the CIS and configuration registers.
	True IDE Mode			In this mode, this input signal is not used and should be connected to VCC by the host.
OE#		I	9	Output Enable Input
	PC Card Memory Mode			This is a strobe generated by the host interface. It is used to read data from the PC Card and to read the CIS and configuration registers.
	PC Card I/O Mode			This signal is used to read the CIS and configuration registers.
	True IDE Mode			To enable the True IDE Mode, this input should be grounded by the host.
		I	7, 42	Card Enable Inputs
CE1#, CE2#	PC Card Memory Mode			These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the odd byte of the word. CE1# accesses the even byte or the odd byte of the word depending on A0 and CE2#. A multiplexing scheme based on A0, CE1#, CE2# allows 8 bit hosts to access all data on D0~D7.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
CS0#, CS1#	True IDE Mode			In the True IDE Mode, CS0# is the chip select for the task file registers while CS1# is used to select the Alternate Status Register and the Device Control Register.
		O	33	Write Protect / I/O Port 16 Output
WP	PC Card Memory Mode			The card does not have a WP switch. This signal is held low after reset initialization

				sequence.
IOIS16#	PC Card I/O Mode			A low signal indicated that a 16 bit or odd byte only operation can be performed.
IOCS16#	True IDE Mode			This signal is asserted low when the card is expecting a word data transfer cycle.
GND		Power	1,34, 35,68	Ground Pin
Vcc		Power	17, 51	Power Supply Pin (5.0V/3.3V)
		I	58	Card Reset Input
RESET	PC Card Memory Mode			When this pin is high, this signal resets the Flash Card. The card Reset is only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
RESET#	True IDE Mode			In this mode, this input pin is the active low from the host.
		I	61	Attribute Memory Select Input
REG#	PC Card Memory Mode			This signal is used to select between Register/ Attribute Memory (REG# = low) and Common Memory (REG# = high).
REG#	PC Card I/O Mode			Active Low on this signal will allow accesses to I/O space
DMACK#	True IDE Mode			This is a DMA Acknowledge signal that is asserted by the host in response to DREQ to initiate DMA transfers.
		O	16	Ready/Interrupt Request Output
RDY/BSY#	PC Card Memory Mode			This signal is set high when the card is ready to accept a new data transfer operation and held low when the card is busy. The host must have a pullup resistor on this signal. When powering-up and when reset
IREQ#	PC Card I/O Mode			In this mode, this signal is used as for interrupt request. This line is strobed low to

				generate a pulse mode interrupt or held low for a level mode interrupt. This is set using Configuration Option Register.
INTRQ	True IDE Mode			In this mode, the signal is active high request to the host.
		O	60	Input Port Acknowledge Output
INPACK#	PC Card Memory Mode			This signal is not used in this mode.
INPACK#	PC Card I/O Mode			This signal is asserted by the card when the card is selected and is responding to an I/O read cycle. This signal is used by the host to enable the input data buffers between the host and the card.
DREQ	True IDE Mode			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host.
CSEL#		I	56	Cable Select Input
	PC Card Memory Mode			This signal is not used in this mode.
	PC Card I/O Mode			This signal is not used in this mode.
	True IDE Mode			This signal is used to configure this device as Master or Slave. When this pin is grounded, this device is configured as Master. When this pin is tied to VCC this card is configured as Slave.
		O	59	Extend Bus Cycle/I/O Channel Ready Output
WAIT#	PC Card Memory Mode			This signal is driven low by the card to inform the host to delay completion of the cycle in progress.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
WAIT#	True IDE Mode			This signal is negated to extend the host transfer cycle of any host register access (rear or write) when the card is not ready to respond to a data transfer request. When not negated, the signal is in high-impedance state.
VS1#,		O	43, 57	Voltage Sense Outputs

VS2#	All Modes			VS1# is grounded so that the Card's CIS can be read at 3.3V and VS2# is left open.
D15~D0		I/O	41,40,39,38,37,66,65,64,6,5,4,3,2,32,31,30	16-bit Data Input/output Bus
	PC Card Memory Mode			These lines carry the Data, Commands, and Status Information between the host and the controller. D15 is the MSB of odd byte and D7 the MSB of even byte in a Word Access.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
	True IDE Mode			All task file operations occur in byte mode on D7~D0, while all data transfers are word (16-bit) accesses.
A10~A0		I	8,11,12,22,23,24,25,26,27,28,29	Card Address Input Bus
	PC Card Memory Mode			These addresses along with the REG# signal are used to select the following: the I/O port address registers within the card, the memory mapped port address registers, a byte in the CIS and Configuration Control and Status registers.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
A2~A0	True IDE Mode	I	27,28,29	In this mode, only A2~A0 are used to select one of the eight Task File registers. All the remaining unused addresses should be grounded by the host.
		O	63	Battery Voltage Detect Output / Card Status Changed Output / Passed Diagnostics

				Input/output
BVD1	PC Card Memory Mode			This signal is asserted high since the card does not contain a battery.
STSCHG#	PC Card I/O Mode			This signal is asserted low to alert the host to changes in the RDY/BSY# and Write Protect states. Its use is controlled through the Card Configuration and Status Registers.
PDIAG#	True IDE Mode	I/O		This signal is asserted by slave drive to indicate to master drive that it has completed diagnostics and is ready to provide status.
		O	62	Battery Voltage Detect Output / Audio Waveform Output / Drive Active/Drive 1 Preset Output
BVD2	PC Card Memory Mode			This signal is asserted high since the card does not contain a battery.
SPKR#	PC Card I/O Mode			This signal is asserted high since the card does not support audio.
DASP#	True IDE Mode	I/O		This signal indicates that a drive is active or that a slave drive (Drive 1) is present.

6. Power Management

AFAYA PCMCIA-ATA Flash Card provides automatic Power saving Mode.

1. Standby Mode: When PCMCIA-ATA Flash Card finished initialization after power reset or hardware reset, it goes into Standby Mode to wait for Command In or Soft Reset.

2. Active Mode: If PCMCIA-ATA Flash Card received any Command In or Soft Reset, it goes into Active Mode. In Active Mode, it is capable of executing any ATA commands. The power consumption is the greatest in this mode.

3. Sleep Mode: The PCMCIA-ATA Flash Card will enter Sleep Mode if there is no Command In or Soft Reset from the host for about 4ms or sleep command is asserted. This time interval can be modified by firmware if necessary. Sleep Mode provides the lowest power consumption. During Sleep Mode, the system main clock is stopped. This mode can be waked up from hardware reset, software reset or any ATA command asserted.

7. Electrical Specification

The following table defines all D.C. Characteristics for the AFAYA. The conditions are:

Commercial Temperature Products
V_{CC} = 5V ±10% V_{CC} = 3.3V ± 5% Ta = 0°C to 70°C

7.1. Power Pin Description

Pin Name	I/O	Description
V_{CCk}	Power	Host V_{CC}
V_{CC} 3.3V	Power	3.3V V_{CC}
GND	Power	GND

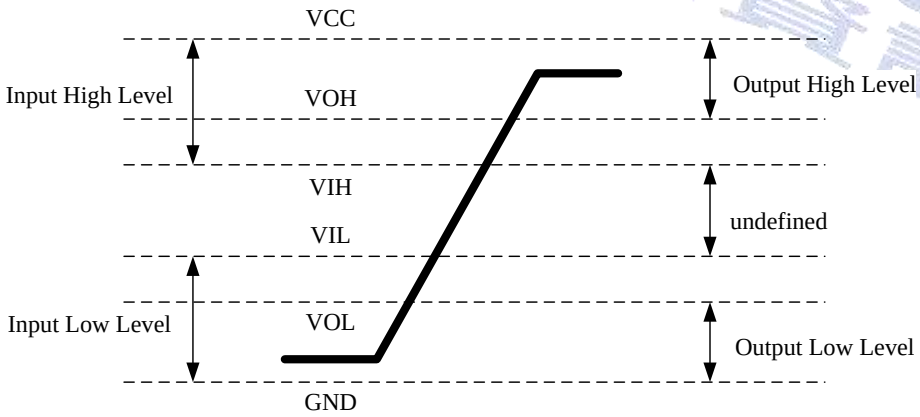
6.1. Absolute Maximum Rating

6.1.1. PCMCIA-ATA FLASH CARD interface I/O at 5.0V

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Power Supply	4.5	5.5	V
V_{OH}	Output Voltage High Level	V_{CC}-0.8		V
V_{OL}	Output Voltage Low Level		0.8	V
V_{IH}	Input Voltage High Level	2.92		V
V_{IL}	Input Voltage Low Level		1.7	V
T_{OPR-W}	Operating temperature for wide grade	-40	+85	℃
T_{OPR-S}	Operating temperature for standard grade	0	+70	℃
T_{STG}	Storage temperature	-40	125	℃

6.1.2. PCMCIA-ATA FLASH CARD interface I/O at 3.3V

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Power Supply	2.97	3.63	V
V_{OH}	Output Voltage High Level	V_{CC}-0.8		V
V_{OL}	Output Voltage Low Level		0.8	V
V_{IH}	Input Voltage High Level	2.05		V
V_{IL}	Input Voltage Low Level		1.25	V
T_{OPR-W}	Operating Temperature For Wide Grade	-40	+85	℃
T_{OPR-S}	Operating Temperature For Standard Grade	0	+70	℃
T_{STG}	Storage Temperature	-40	125	℃



6.1.3. The I/O pins other than PCMCIA-ATA FLASH CARD interface

Symbol	Parameter	Min.	Max.	Unit	Remark
V_{CC}	Supply Voltage	2.7	3.6	V	
V_{OH}	High level output voltage	2.4		V	
V_{OL}	Low level output voltage		0.4	V	
V_{IH}	High level input voltage	2.0		V	Non-Schmitt trigger
		1.4	2.0	V	Schmitt trigger3
V_{IL}	Low level input voltage		0.8	V	Non-Schmitt trigger
		0.8	1.2	V	Schmitt trigger3

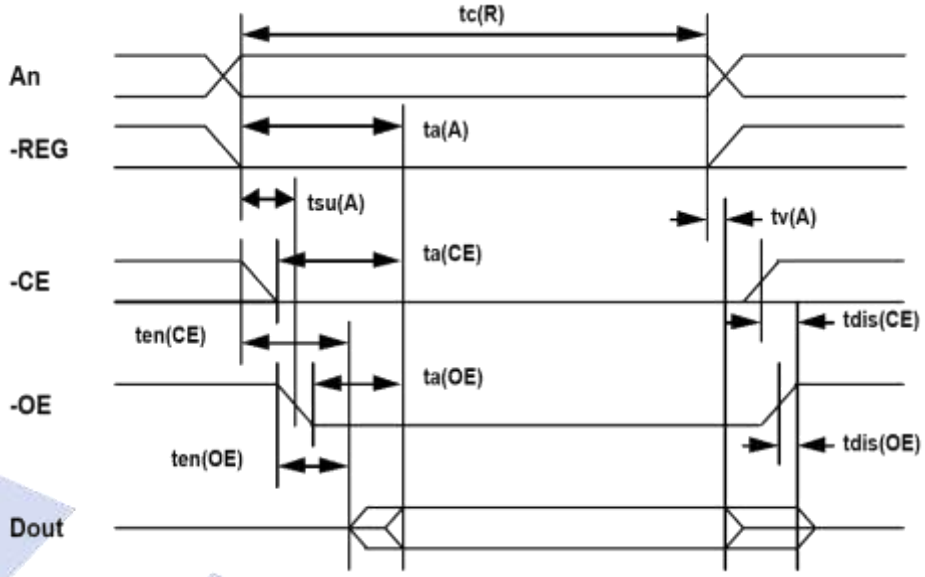
6.2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IN}	Input Voltage	-0.3	-	V_{CC} +0.3	V
Vccq	Power Supply for Host I/O	3.0	-	5.5	V
V_{IN_Host}	Input Voltage for Host I/O	-0.3	-	Vccq +0.3	V

6.3. AC Characteristics

6.3.1. Attribute Memory Read Timing

Speed Version			**300 ns**	
Symbol	**Item**	**IEEE Symbol**	**Min**	**Max**
tc(R)	Read Cycle Time	tAVAV	300	
ta(A)	Address Access Time	tAVQV		300
ta(CE)	Card Enable Access Time	tELQV		300
ta(OE)	Output Enable Access Time	tGLQV		150
tdis(CE)	Output Disable Time from CE	tEHQZ		100
tdis(OE)	Output Disable Time from OE	tGHQZ		100
tsu (A)	Address Setup Time	tAVGL	30	
ten(CE)	Output Enable Time from CE	tELQNZ	5	
ten(OE)	Output Enable Time from OE	tGLQNZ	5	
tv(A)	Data Valid from Address Change	tAXQX	0	



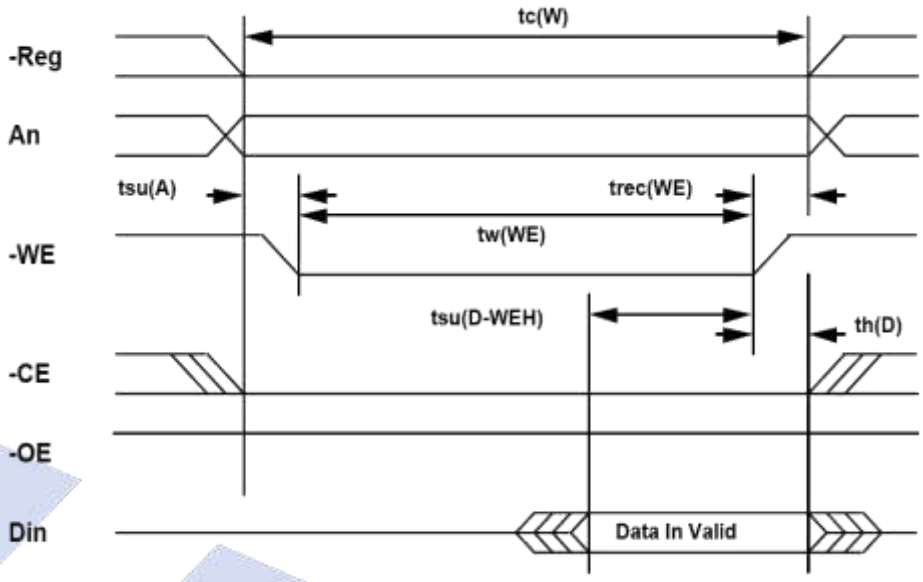
Attribute Memory Read Timing Diagram

6.3.2. Configuration Register (Attribute Memory) Write Timing

Speed Version			250 ns	
Symbol	**Item**	**IEEE Symbol**	**Min**	**Max**
tc(W)	Write Cycle Time	tAVAV	250	
tw(WE)	Write Pulse Width	tWLWH	150	
tsu(A)	Address Setup Time	tAVWL	30	
trec(WE)	Write Recovery Time	tWMAX	30	
tsu(D-WEH)	Data Setup Time for WE	tDVWH	80	
th(D)	Data Hold Time	tWMDX	30	

Note:

All times are in nanoseconds. Din signifies data provided by the system to the PCMCIA-ATA FLASH CARD.



Configuration Register (Attribute Memory) Write Timing Diagram

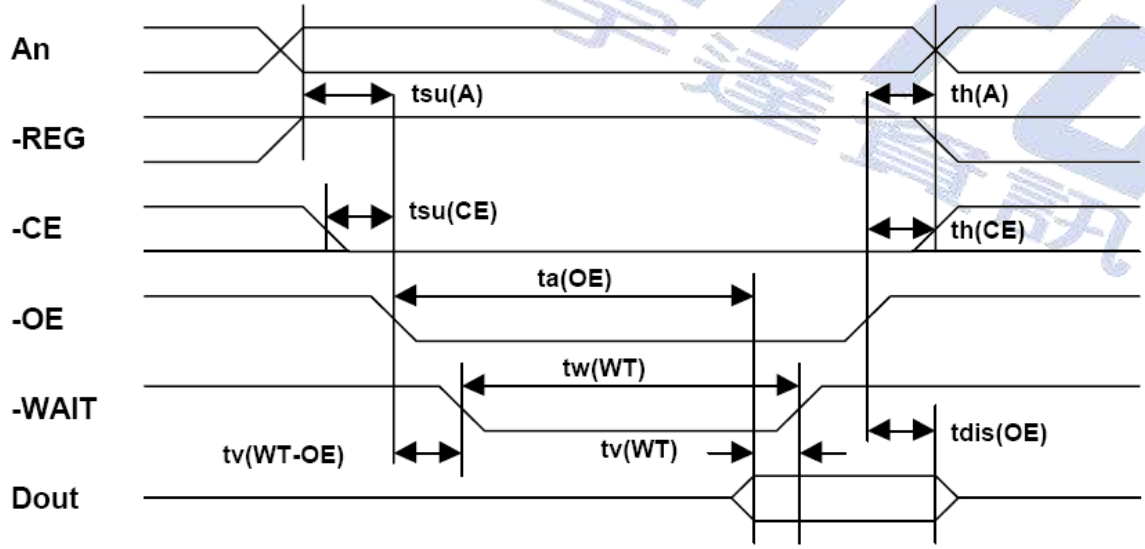
6.3.3. Common Memory Read Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Symbol	Item	IEEE Symbol	Min	Max	Min	Max	Min	Max	Min	Max
ta(OE)	Output Enable Access Time	tGLQV		125		60		50		45
Tdis(OE)	Output Disable Time from OE	tGHQZ		100		60		50		45
tsu(A)	Address Setup Time	tAVGL	30		15		10		10	
th(A)	Address Hold Time	tGHAX	20		15		15		10	
tsu(CE)	CE Setup before OE	tELGL	0		0		0		0	
th(CE)	CE Hold following OE	tGHEH	20		15		15		10	
tv(WT-OE)	Wait Delay Falling from OE	tGLWTV		35		35		35		na[1]
tv(WT)	Data Setup for Wait Release	tQVWTH		0		0		0		na[1]
tw(WT)	Wait Width Time[2]	tWTLWTH		350		350		350		na[1]

Note:

1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the PCMCIA-ATA FLASH CARD. to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.



Common Memory Read Timing Diagram

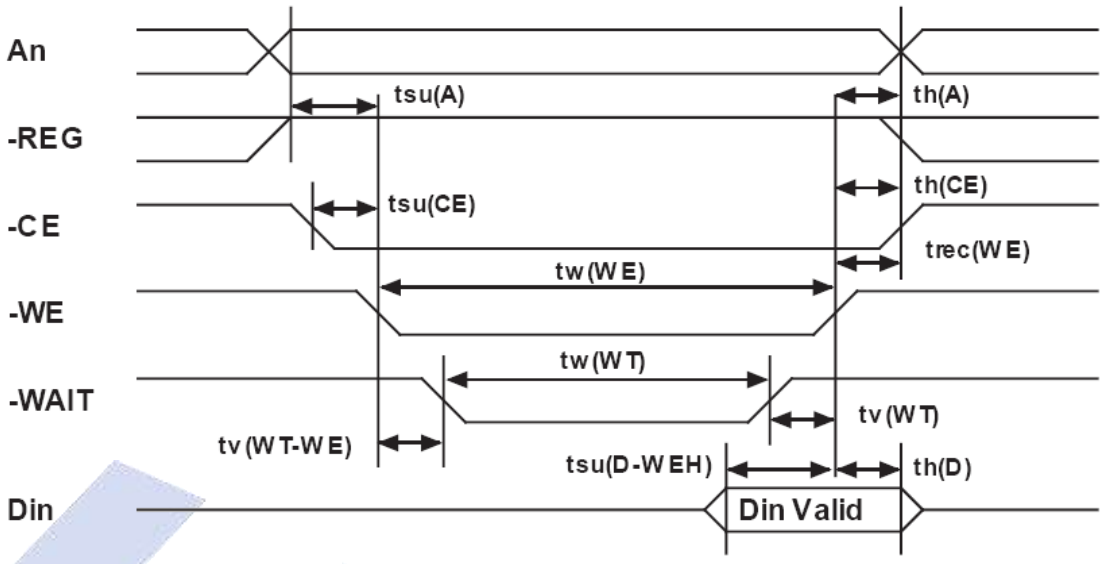
6.3.4. Common Memory Write Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Symbol	Item	IEEE Symbol	Min	Max	Min	Max	Min	Max	Min	Max
tsu (D-WEH)	Data Setup before WE	tDVWH	80		50		40		30	
th (D)	Data Hold following WE	tWMDX	30		15		10		10	
tw (WE)	WE Pulse Width	tWLWH	150		70		60		55	
tsu (A)	Address Setup Time	tAVWL	30		15		10		10	
tsu (CE)	CE Setup before WE	tELWL	0		0		0		0	
trec (WE)	Write Recovery Time	tWMAX	30		15		15		15	
th (A)	Address Hold Time	tGHAX	20		15		15		15	
th (CE)	CE Hold following WE	tGHEH	20		15		15		10	
tv (WT-WE)	Wait Delay Falling from WE	tWLWTV		35		35		35		na[1]
tv (WT)	WE High from Wait Release	tWTHWH	0		0		0		na[1]	
tw (WT)	Wait Width Time[2]	tWTLWTH		350		350		350		na[1]

Note:

1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the PCMCIA-ATA FLASH CARD. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.



Common Memory Write Timing Diagram

6.3.5. I/O Read Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Symbol	Item	IEEE Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Td (IORD)	Data Delay after IORD	tIGLQV		100		50		45		45
Th (IORD)	Data Hold following IORD	tIGHQX	0		5		5		5	
Tw (IORD)	IORD Width Time	tIGLIGH	165		70		65		55	
tsuA (IORD)	Address Setup before IORD	tAVIGL	70		25		25		15	
thA (IORD)	Address Hold following IORD	tIGHAX	20		10		10		10	
tsuCE (IORD)	CE Setup before IORD	tELIGL	5		5		5		5	
thCE (IORD)	CE Hold following IORD	tIGHEH	20		10		10		10	
tsuREG (IORD)	REG Setup before IORD	tRGLIGL	5		5		5		5	
thREG (IORD)	REG Hold following IORD	tIGHRGH	0		0		0		0	
tdfINPACK (IORD)	INPACK Delay Falling from IORD3	tIGLIAL	0	45	0	na1	0	na1	0	na1
tdrINPACK (IORD)	INPACK Delay Rising from IORD3	tIGHIAH		45		na1		na1		na1
tdfIOIS16 (ADR)	IOIS16 Delay Falling from Address3	tAVISL		35		na1		na1		na1
tdrIOIS16 (ADR)	IOIS16 Delay Rising from Address3	tAVISH		35		na1		na1		na1

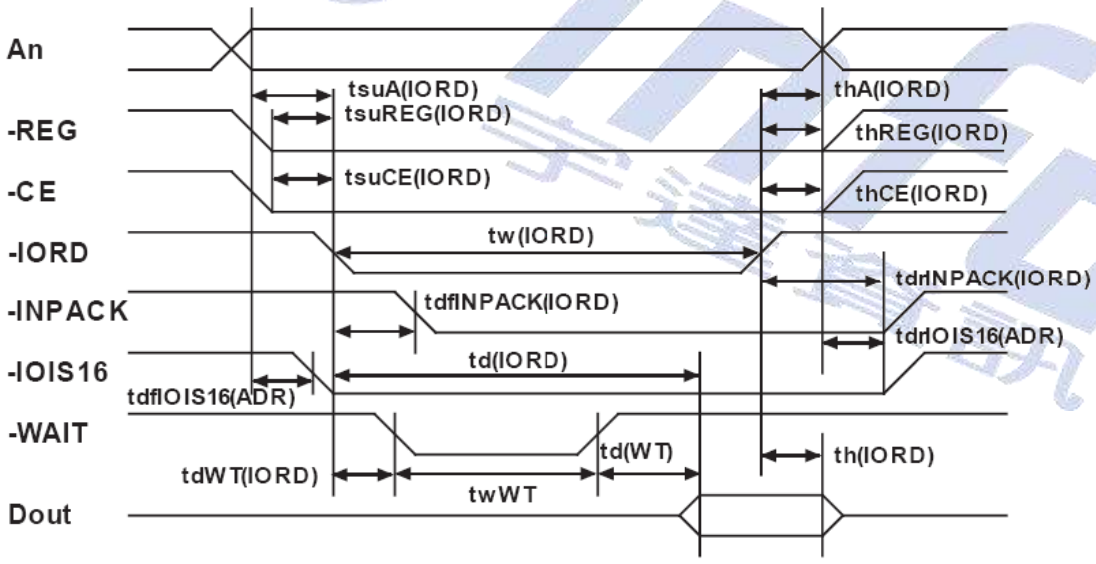
Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Symbol	Item	IEEE Symbol	Min	Max	Min	Max	Min	Max	Min	Max
tdWT (IORD)	Wait Delay Falling from IORD3	tIGLWTL		35		35		35		na2
Td (WT)	Data Delay from Wait Rising3	tWTHQV		0		0		0		na2
Tw (WT)	Wait Width Time3	tWTLWTH		350		350		350		na2

Note:

(1) -IOIS16 and -INPACK are not supported in this mode.

(2) -WAIT is not supported in this mode.

(3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the PCMCIA-ATA FLASH CARD to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.



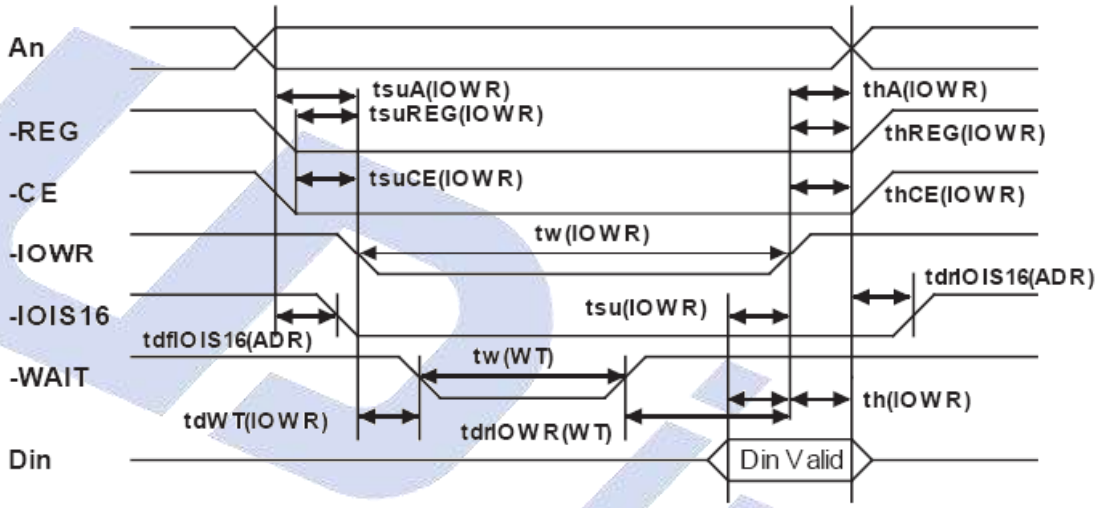
I/O Read Timing Diagram

6.3.6. I/O Write Timing

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Symbol	Item	IEEE Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Tsu (IOWR)	Data Setup before IOWR	tDVIWH	60		20		20		15	
Th (IOWR)	Data Hold following IOWR	tlWHDX	30		10		5		5	
Tw (IOWR)	IOWR Width Time	tlWLIWH	165		70		65		55	
tsuA (IOWR)	Address Setup before IOWR	tAVIWL	70		25		25		15	
thA (IOWR)	Address Hold following IOWR	tlWHAX	20		20		10		10	
tsuCE (IOWR)	CE Setup before IOWR	tELIWL	5		5		5		5	
thCE (IOWR)	CE Hold following IOWR	tlWHEH	20		20		10		10	
tsuREG (IOWR)	REG Setup before IOWR	tRGLIWL	5		5		5		5	
thREG (IOWR)	REG Hold following IOWR	tlWHRGH	0		0		0		0	
tdfIOIS16 (ADR)	IOIS16 Delay Falling from Address[3]	tAVISL		35		na[1]		na[1]		na[1]
tdrIOIS16 (ADR)	IOIS16 Delay Rising from Address[3]	tAVISH		35		na[1]		na[1]		na[1]
tdWT (IOWR)	Wait Delay Falling from IOWR[3]	tlWLWTL		35		35		35		na[2]
tdrIOWR (WT)	IOWR high from Wait high[3]	tWTJIWH	0		0		0		na[2]	
Tw (WT)	Wait Width Time[3]	tWTLWTH		350		350		350		na[2]

Note:

1) *-IOIS16 and -INPACK are not supported in this mode.*
2) *-WAIT is not supported in this mode.*
3) *The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the PCMCIA-ATA FLASH CARD. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.*



I/O Write Timing Diagram

6.3.7. True IDE PIO Mode Read/Write Timing

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t_0	Cycle time (min)[1]	600	383	240	180	120	100	80
t_1	Address Valid to HIOE/HIOW setup (min)	70	50	30	30	25	15	10
t_2	HIOE/HIOW (min)[1]	165	125	100	80	70	65	55
t_2	HIOE/HIOW (min) Register (8 bit)[1]	290	290	290	80	70	65	55
t_{2i}	HIOE/HIOW recovery time (min)[1]	-	-	-	70	25	25	20
t_3	HIOW data setup (min)	60	45	30	30	20	20	15
t_4	HIOW data hold (min)	30	20	15	10	10	5	5
t_5	HIOE data setup (min)	50	35	20	20	20	15	10
t_6	HIOE data hold (min)	5	5	5	5	5	5	5
t_{6Z}	HIOE data tristate (max)[2]	30	30	30	30	30	20	20
t_7	Address valid to IOCS16 assertion (max)[4]	90	50	40	n/a	n/a	n/a	n/a
t_8	Address valid to IOCS16 released (max)[4]	60	45	30	n/a	n/a	n/a	n/a
t_9	HIOE/HIOW to address valid hold	20	15	10	10	10	10	10
t_{RD}	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0
t_A	IORDY Setup time[3]	35	35	35	35	35	na[5]	na[5]
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na[5]	na[5]
t_C	IORDY assertion to release (max)	5	5	5	5	5	na[5]	na[5]

Note:

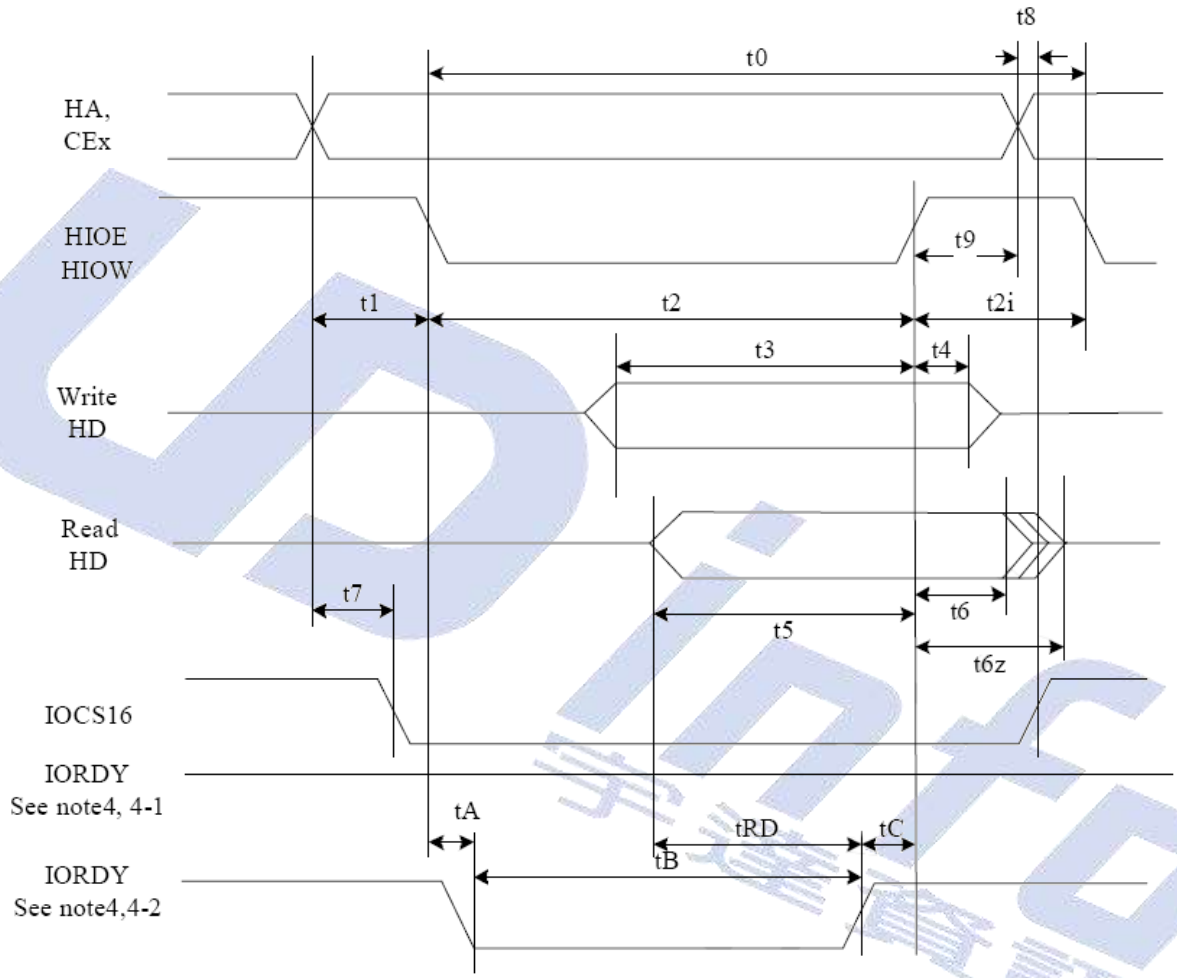
All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

1) *t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A PCMCIA-ATA FLASH CARD implementation shall support any legal host implementation.*
2) *This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the PCMCIA-ATA FLASH CARD (tri-state).*
3) *The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is*

inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the PCMCIA-ATA FLASH CARD is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the PCMCIA-ATA FLASH CARD is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

5) IORDY is not supported in this mode.



True IDE PIO Mode Timing Diagram

Notes:

(1) Device address consists of CE0, CE1, and HA[2:0]

(2) Data consists of HD[15:00] (16-bit) or HD[7:0] (8 bit)

(3) IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of HIOE or HIOW. The assertion and negation of IORDY is described in the following three cases:

(4-1) Device never negates IORDY: No wait is generated.

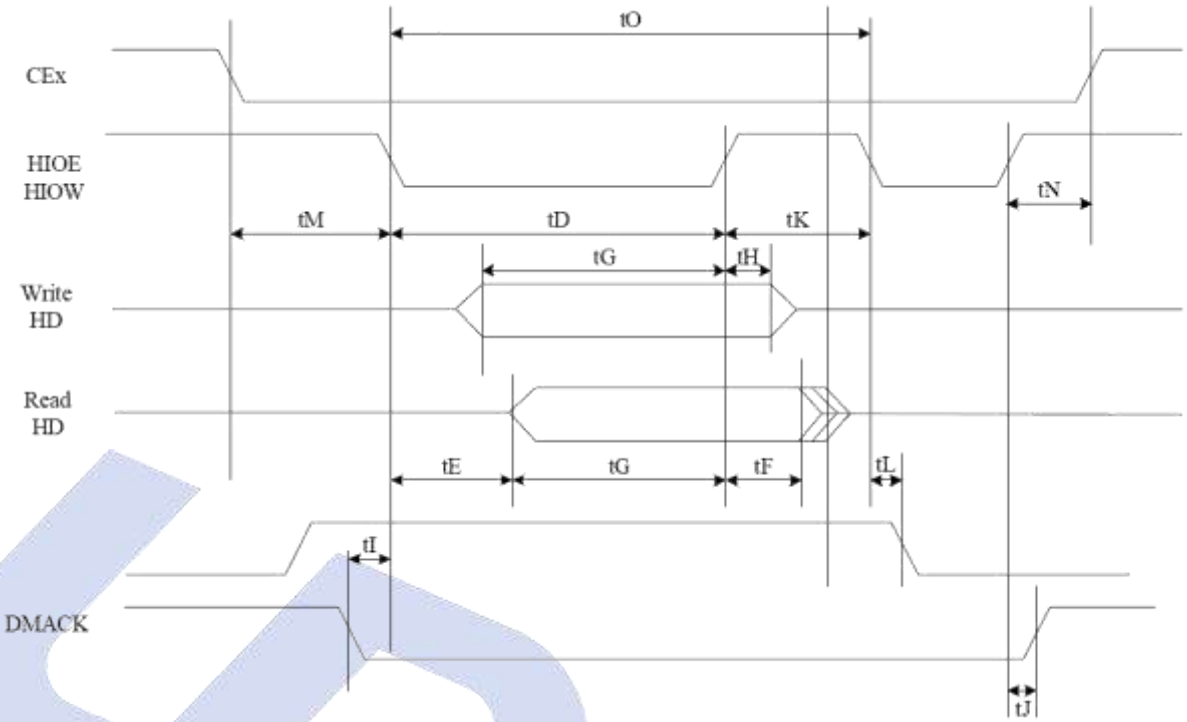
(4-2) Device drives IORDY low before t_A: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and HIOE is asserted, the device shall place read data on D15-D00 for t_{RD} before causing IORDY to be asserted.

6.3.8. True IDE Multiword DMA Mode Read/Write Timing

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
t_O	Cycle time (min)	480	150	120	100	80	1
t_D	HIOE / HIOW asserted width (min)	215	80	70	65	55	1
t_E	HIOE data access (max)	150	60	50	50	45	
t_F	HIOE data hold (min)	5	5	5	5	5	
t_G	HIOE/HIOW data setup (min)	100	30	20	15	10	
t_H	HIOW data hold (min)	20	15	10	5	5	
t_I	DMACK(HREG) to HIOE/HIOW setup (min)	0	0	0	0	0	
t_J	HIOE / HIOW to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	HIOE negated width (min)	50	50	25	25	20	1
t_{KW}	HIOW negated width (min)	215	50	25	25	20	1
t_{LR}	HIOE to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	HIOW to DMARQ delay (max)	40	40	35	35	35	
t_M	CEx valid to HIOE / HIOW	50	30	25	10	5	
t_N	CEx hold	15	10	10	10	10	

Notes:

T0 is the minimum total cycle time and tD is the minimum command active time, while tKR and tKW are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tKR, and tKW shall be met. The minimum total cycle time requirement is greater than the sum of tD and tKR or tKW.for input and output cycles respectively. This means a host implementation can lengthen either or both of tD and either of tKR, and tKW as needed to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A PCMCIA-ATA FLASH CARD implementation shall support any legal host implementation.



True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:

1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

2) This signal may be negated by the host to suspend the DMA transfer in progress.

6.3.9. Ultra DMA Signal Usage In Each Interface Mode

Signal	Type	(Non UDMA MEM MODE)	PC CARD MEM MODE UDMA	PC CARD IO MODE UDMA	TRUE IDE MODE UDMA
DMARQ	Output	(-INPACK)	-DMARQ	-DMARQ	DMARQ
HREG	Input	(-REG)	-DMACK	DMACK	-DMACK
HIOW	Input	(-IOWR)	STOP[1]	STOP[1]	STOP[1]
HIOE	Input	(-IORD)	-HDMARDY(R) [1,2] HSTROBE(W) [1, 3, 4]	-HDMARDY(R) [1, 2] HSTROBE(W) [1, 3, 4]	-HDMARDY(R) [1, 2] HSTROBE(W)[1, 3, 4]
IORDY	Output	(-WAIT)	-DDMARDY (W) [1, 3] DSTROBE(R) [1. 2. 4]	-DDMARDY (W) [1, 3] DSTROBE(R) [1. 2. 4]	-DDMARDY (W) [1, 3] DSTROBE(R) [1. 2. 4]
HD[15:00]	Bidir	(D[15:00])	D[15:00]	D[15:00]	D[15:00]
HA[10:00]	Input	(A[10:00])	A[10:00]	A[10:00]	A[02:00] [5]
CSEL	Input	(-CSEL)	-CSEL	-CSEL	-CSEL
HIRQ	Output	(READY)	READY	-INTRQ	INTRQ
CE1 CE2	Input	(-CE1) (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Notes:

1) *The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.*
2) *The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.*
3) *The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.*
4) *The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.*
5) *Address lines 03 through 10 are not used in True IDE mode.*

6.3.10. Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		Measure Location[2]
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		40		Sender
t_{CYC}	112		73		54		39		25		16.8		Note3
t_{2CYC}	230		153		115		86		57		38		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		Host
t_{ZFS}	0		0		0		0		0		35		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		Sender
t_{FS}		230		200		170		130		120		90	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	Note4
t_{MLI}	20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10	Note5
t_{ZAH}	20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	Host
t_{RFS}		75		70		60		60		60		50	Sender
t_{RP}	160		125		100		100		100		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		Sender

Notes:

All Timings in ns

1) *All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.*
2) *All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and –DMARDY transitions are measured at the sender connector.*
3) *The parameter tCYC shall be measured at the recipient's connector farthest from the sender.*
4) *The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.*
5) *The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.*
6) *See the AC Timing requirements in Table 28: Ultra DMA AC Signal Requirements.*

6.3.11. Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data outburst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
Name	Comment	Notes
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	

t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

(1) The parameters t_{UI}, t_{MLI} (in 6.4.17: Ultra DMA Data-In Burst Device Termination Timing and 6.4.18: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

(2) 80-conductor cabling (see ATA specification :Annex A) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

(3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

1) For all timing modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

6.3.12. Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		UDMA Mode 5		UDMA Mode 6	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		2.3		4.8		2.3		2.3	
t_{DHIC}	4.8		4.8		4.8		2.8		4.8		2.8		2.8	
t_{DVSIC}	72.9		50.9		33.9		6.0		9.5		6.0		5.2	
t_{DVHIC}	9.0		9.0		9.0		6.0		9.0		6.0		5.2	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)													
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)													
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)													
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)													

Notes:

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).

3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

6.3.13. Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
SRISE	Rising Edge Slew Rate for any signal		1.25	1
SFALL	Falling Edge Slew Rate for any signal		1.25	1

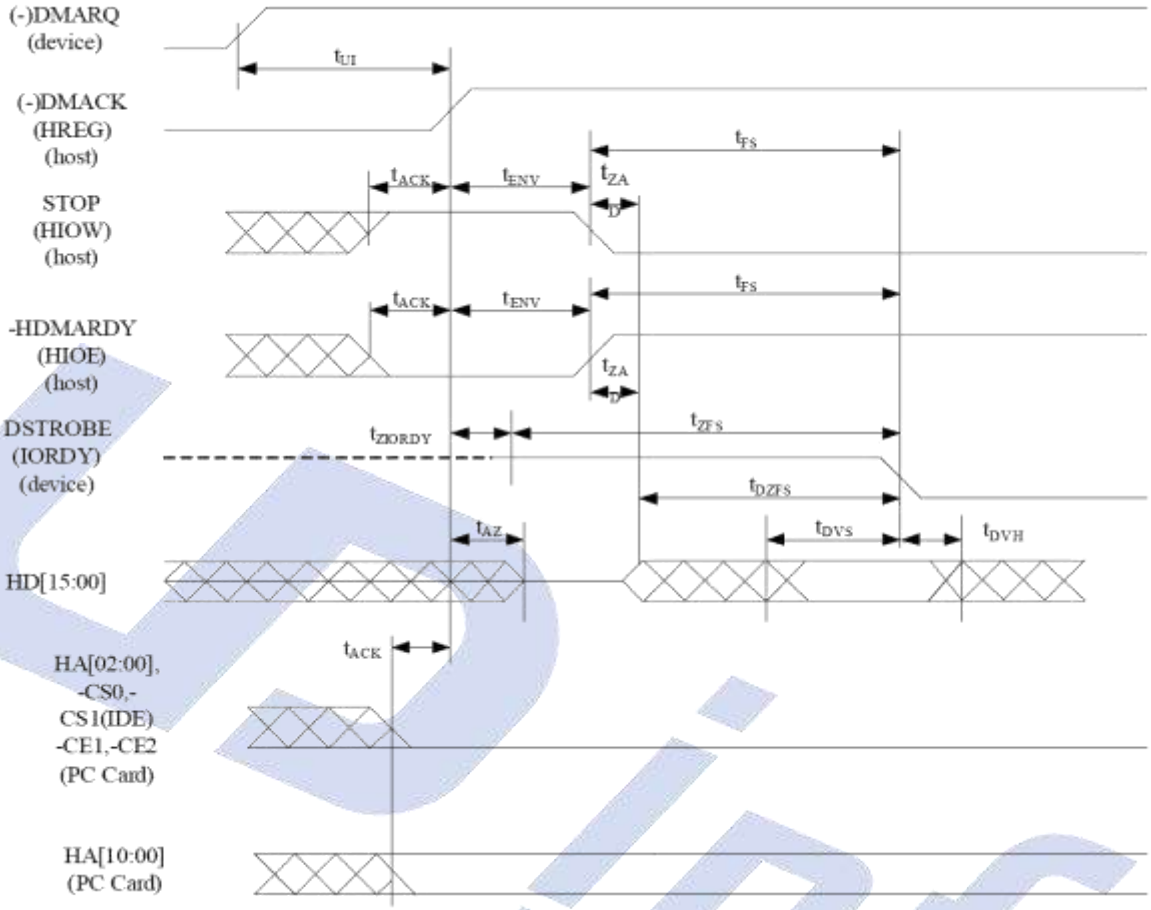
Notes:

1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

6.3.14. Ultra DMA Data-In Burst Initiation Timing



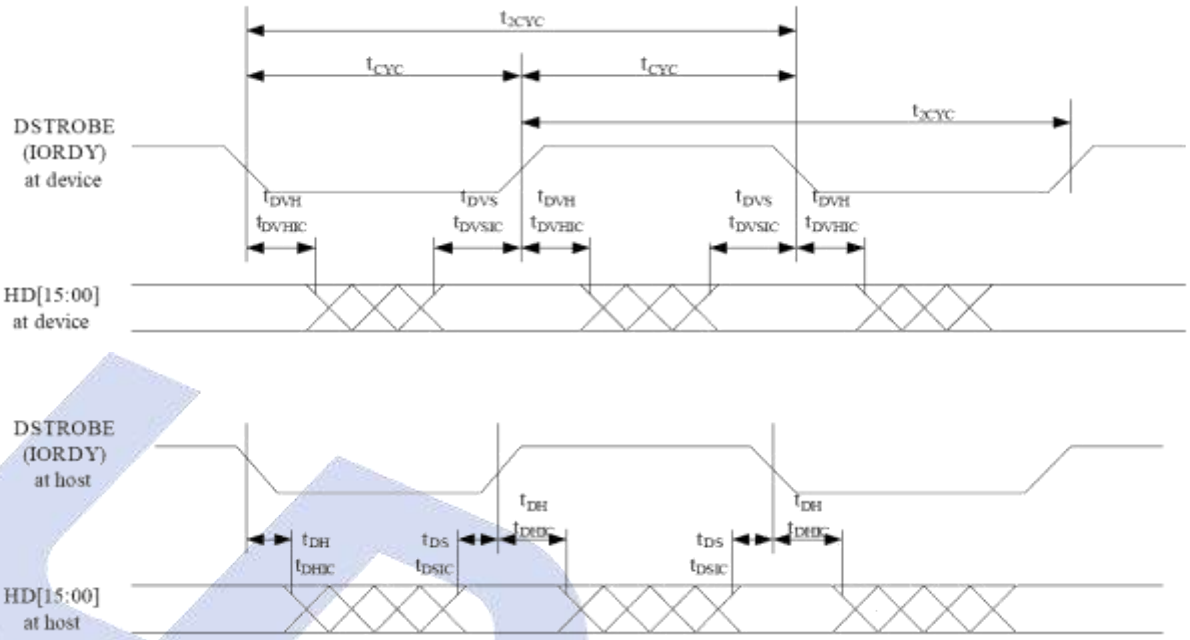
Ultra DMA Data-In Burst Initiation Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

The definitions for the IORDY:-DDMARDY: DSTROBE,-IORD:-HDMARDY: HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted. HA [02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA [10:00], -CE1 and -CE2 are PC Card mode signals. The Bus polarity of (-) DMACK and (-) DMARQ are dependent on interface mode active.

6.3.15. Sustained Ultra DMA Data-In Burst Timing

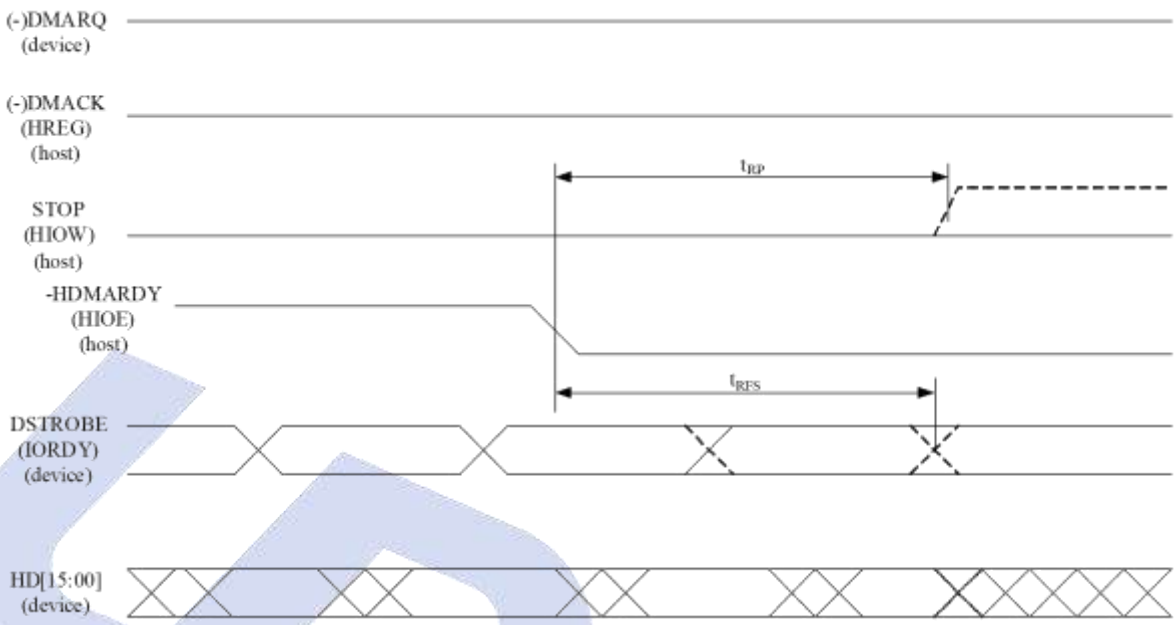


Sustained Ultra DMA Data-In Burst Timing Diagram

Notes:

HD[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until sometime after they are driven by the device.

6.3.16. Ultra DMA Data-In Burst Host Pause Timing



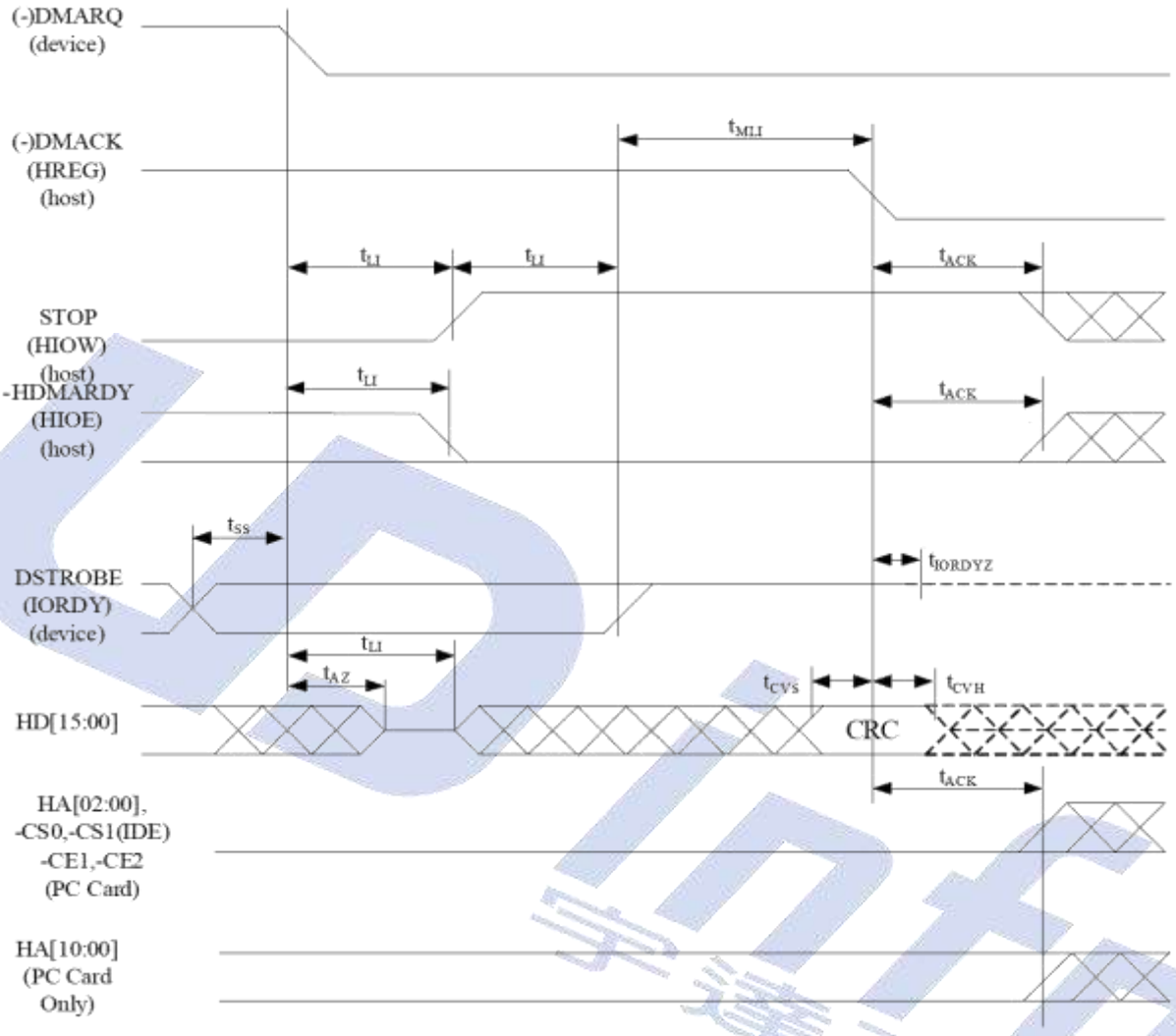
Ultra DMA Data-In Burst Host Pause Timing Diagram

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Notes:

1) *The host may assert STOP to request termination of the Ultra DMA data burst no sooner than tRP after -HDMARDY is negated.*
2) *After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.*
3) *The bus polarity of the (-) DMARQ and (-) DMACK signals is dependent on the active interface mode.*

6.3.17. Ultra DMA Data-In Burst Device Termination Timing



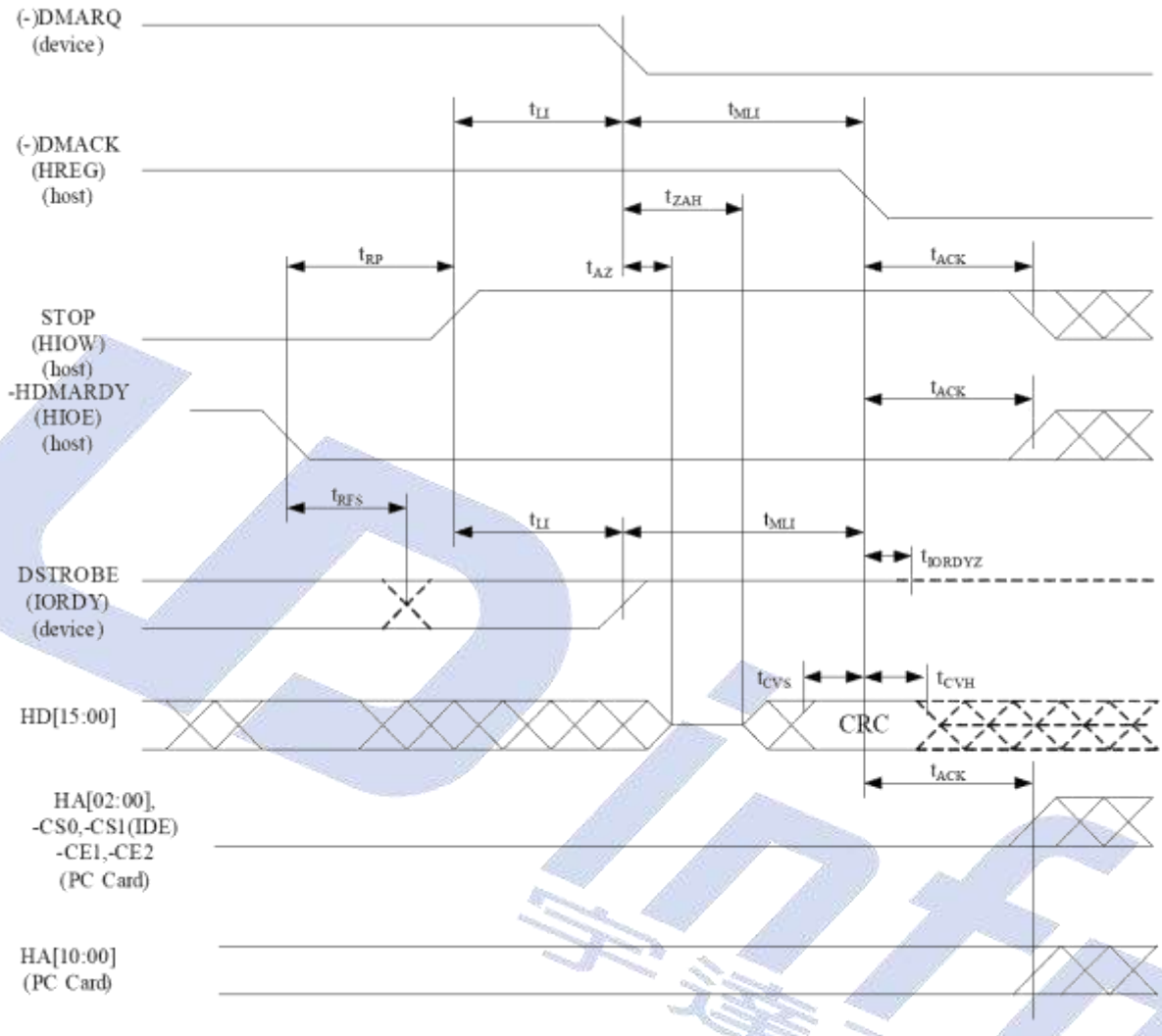
Ultra DMA Data-In Burst Device Termination Timing Diagram

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Notes:

The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA [02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA [10:00], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

6.3.18. Ultra DMA Data-In Burst Host Termination Timing



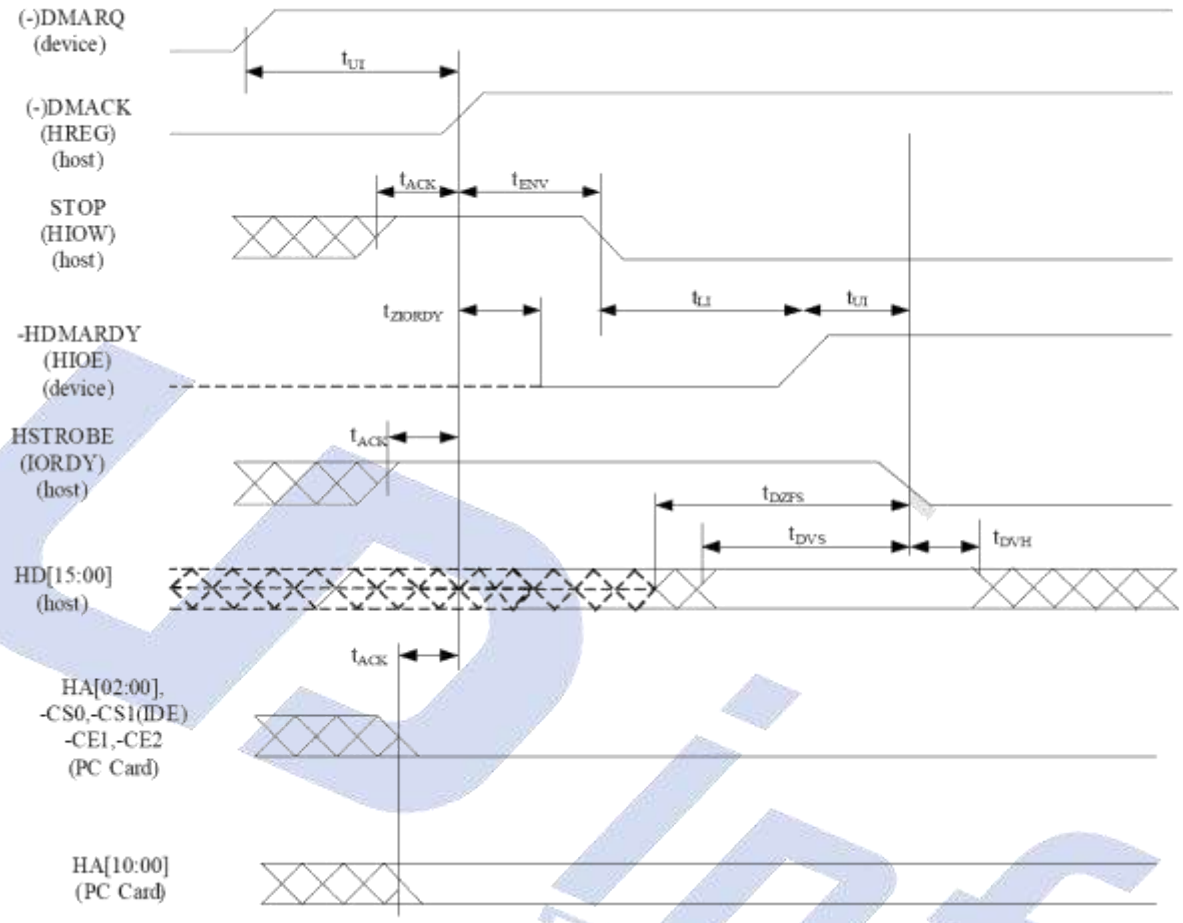
Ultra DMA Data-In Burst Host Termination Timing Diagram

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Notes:

The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA [02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA [10:00],-CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

6.3.19. Ultra DMA Data-Out Burst Initiation Timing



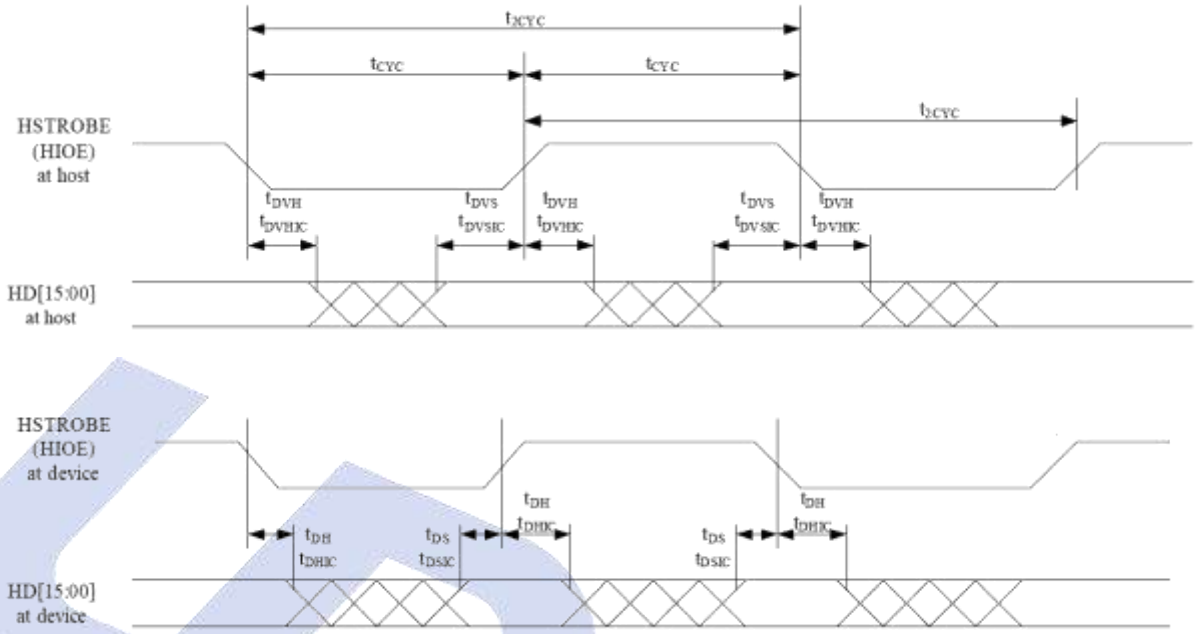
Ultra DMA Data-Out Burst Initiation Timing Diagram

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Note:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted. HA [02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

6.3.20. Sustained Ultra DMA Data-Out Burst Timing

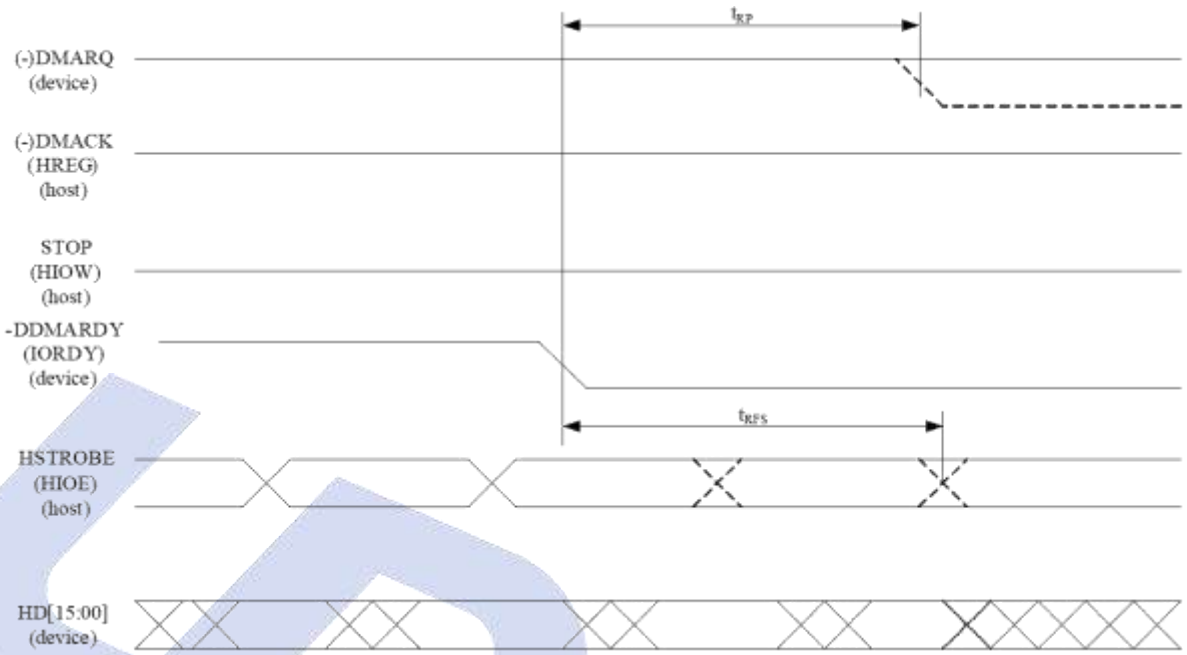


Sustained Ultra DMA Data-Out Burst Timing Diagram

Note:

Data (HD[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until sometime after they are driven by the host.

6.3.21. Ultra DMA Data-Out Burst Device Pause Timing



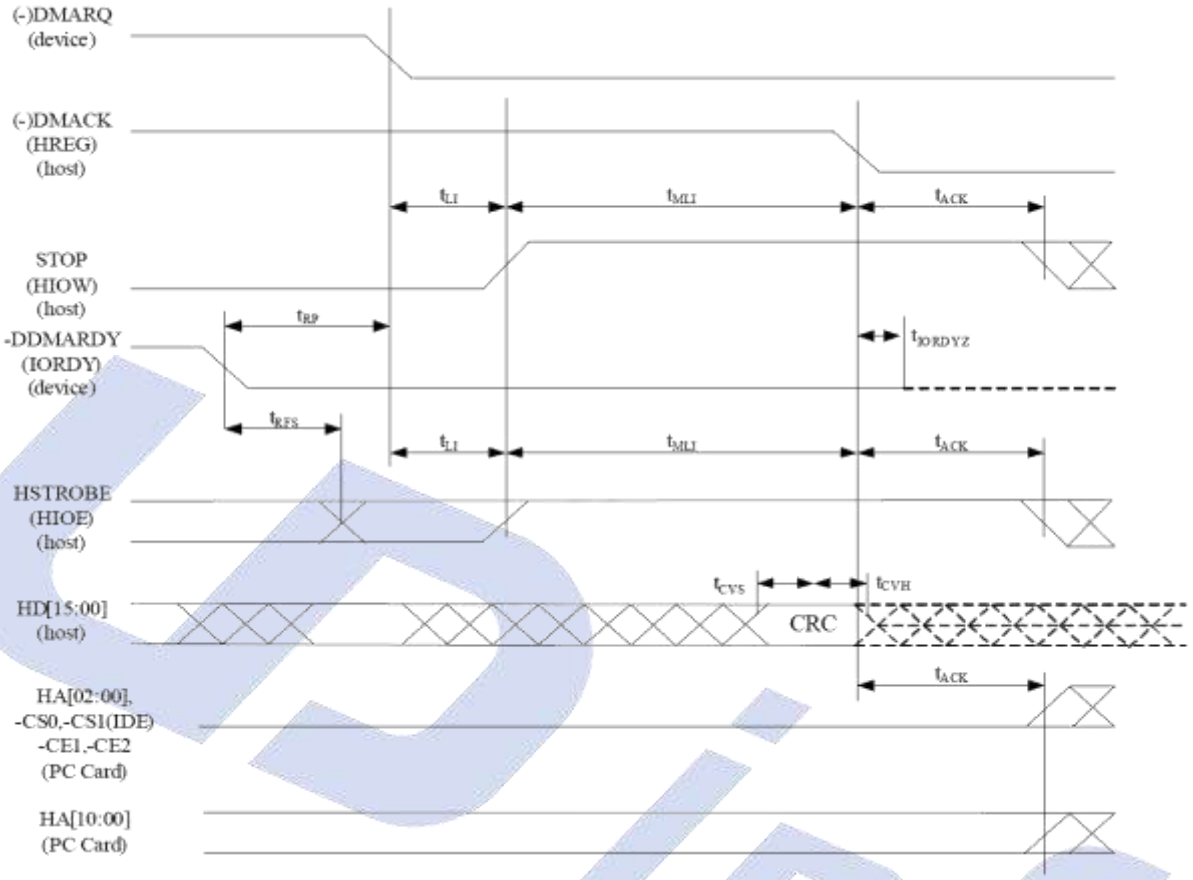
Ultra DMA Data-Out Burst Device Pause Timing Diagram

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Notes:

1) *The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than tRP after -DDMARDY is negated.*
2) *After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.*
3) *The bus polarity of DMARQ and DMACK depend on the active interface mode.*

6.3.22. Ultra DMA Data-Out Burst Device Termination Timing



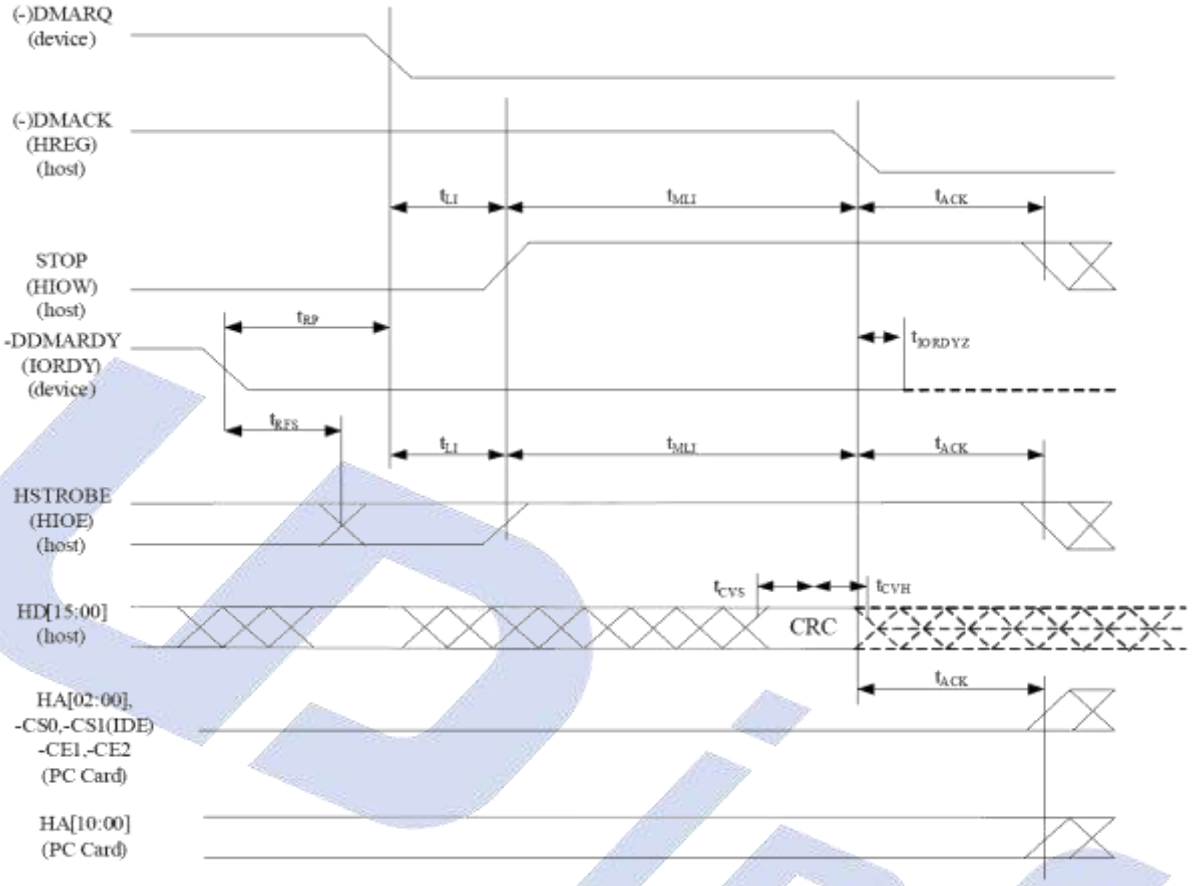
Ultra DMA Data-Out Burst Device Termination Timing Diagram

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Note:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA [02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA [00:10], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK depend on the active interface mode.

6.3.23. Ultra DMA Data-Out Burst Host Termination Timing



Ultra DMA Data-Out Burst Host Termination Timing Diagram

All waveforms in this diagram are shown with the asserted state high. Negative true signals appear inverted on the bus relative to the diagram.

Notes:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA [02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA [10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

5. ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the PCMCIA-ATA Flash Card. Commands are issued to the PCMCIA-ATA Flash Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see ATA Command Set Table) of command

acceptance, all dependent on the host not issuing commands unless the PCMCIA-ATA Flash Card is not busy (BSY=0). All commands listed in this specification shall be implemented.

Commands can be implemented as “no operation” to meet this requirement. The Security Mode feature set (command codes F1, F2, F3, F4, F5, and F6) should not be implemented unless the device is intended to be used in an embedded, non-removable application. The Security Mode feature set was not designed for removable devices and certain problems may be encountered when using these commands in a removable application. This specification introduces some new commands and features. If these commands are used on an older PCMCIA-ATA Flash Card, an Invalid Command Error may occur

7.1. ATA Command Set

Command	Code	FR	SC	SN	CY	DH	LBA	
Check Power Mode	E5 or 98h	–	–	–	–	Y	–	Support
Execute Drive Diagnostic	90h	–	–	–	–	Y	–	Support
Erase Sector	C0h	–	Y	Y	Y	Y	Y	Support
Format Track	50h	–	Y	–	Y	Y	Y	Support
Identify Device	Ech	–	–	–	–	Y	–	Support
Idle	E3h or 97h	–	Y	–	–	Y	–	Support
Idle Immediate	E1h or 95h	–	–	–	–	Y	–	Support
Initialize Drive Parameters	91h	–	Y	–	–	Y	–	Support
NOP	00h	–	–	–	–	Y	–	Support
Read Buffer	E4h	–	–	–	–	Y	–	Support
Read DMA	C8h	–	Y	Y	Y	Y	Y	Support
Read Multiple	C4h	–	Y	Y	Y	Y	Y	Support
Read Sector(s)	20h or 21h	–	Y	Y	Y	Y	Y	Support
Read Verify Sector(s)	40h or 41h	–	Y	Y	Y	Y	Y	Support
Recalibrate	1Xh	–	–	–	–	Y	–	Support
Request Sense	03h	–	–	–	–	Y	–	Support
Seek	7Xh	–	–	Y	Y	Y	Y	Support
Set Feature	EFh	Y	–	–	–	Y	–	Support
Set Multiple Mode	C6h	–	Y	–	–	Y	–	Support
Set Sleep Mode	E6h or 99h	–	–	–	–	Y	–	Support
Standby	E2 or 96h	–	–	–	–	Y	–	Support
Standby Immediate	E0 or 94h	–	–	–	–	Y	–	Support
Translate Sector	87h	–	Y	Y	Y	Y	Y	Support
Wear Level	F5h	–	–	–	–	Y	–	Support
Write Buffer	E8h	–	–	–	–	Y	–	Support
Write DMA	CAh	–	Y	Y	Y	Y	Y	Support
Write Multiple	C5h	–	Y	Y	Y	Y	Y	Support
Write Multiple w/o Erase	CDh	–	Y	Y	Y	Y	Y	Support
Write Sector(s)	30h or 31h	–	Y	Y	Y	Y	Y	Support
Write Sector(s) w/o Erase	38h	–	Y	Y	Y	Y	Y	Support
Write Verify	3Ch	–	Y	Y	Y	Y	Y	Support

Definitions:

FR = Features Register

SC = Sector Count Register (00H-FFH; 00H means 256 sectors)

SN = Sector Number Register

CY = Cylinder Low/High Register

DH = Head No. (0-15) of Drive/Head Register

LBA = Logic Block Address Mode Support

- = Not used for the command

Y = Used for the command

7.2. SMART Command Support

PCMCIA-ATA Flash Card series supports SMART command set and define some vendor specific data to report spare/bad block number in each memory management unit. Users can get the data by "Read Data" command.

SMART Feature Register Values			
D0h	Read Data	D4h	Execute OFF-LINE Immediate
D1h	Read Attribute Threshold	D8h	Enable SMART Operations
D2h	Enable/Disable AutoSaved	D9h	Disable SMART Operations
D3h	Save Attribute Values	DAh	Return Status

Notes: If reserved size below the Threshold, the status can be read from Cylinder register by Return Status command (DAh).

SMART Data Structure (READ DATA (D0h))

BYTE	F / V	Description
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved

		0 1=Device error logging supported
371	X	Vendor specific
BYTE	F / V	Description
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396	V	Number of MU in device (0~n)
397+(n*6)	V	MU number
398+(n*6)	V	MU data block
400+(n*6)	V	MU spare block
401+(n*6)	V	Init. Bad block
402+(n*6)	V	Run time Bad block information
511	V	Data structure checksum

Notes:

F = the content of the byte is fixed and does not change.

V = the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X = the content of the byte is vendor specific and may be fixed or variable.

R = the content of the byte is reserved and shall be zero.

N = Nth Management Unit

** 4 Byte value: [MSB] [2] [1] [LSB]*

7.3. Identify Drive Information(True IDE Mode)

Word Address	Default value	Total Bytes	Data Field Type information
0	848Ah	2	General configuration - signature for the PCMCIA-ATA FLASH CARD
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right Justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	XXXXh	8	Firmware revision in ASCII. Big Endean Byte Order in Word
27-46	XXXXh	40	Model number in ASCII (Left Justified) Big Endean Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0300h	2	Capabilities
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word57=LSW , Word58=MSW)
59	0101h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0007h	2	Multiword DMA transfer. In PCMCIA mode this value shall be oh
64	0003h	2	Advanced PIO modes supported

Word Address	Default value	Total Bytes	Data Field Type information
65	0078h	2	Minimum Multiword DMA transfer cycle time per word.
66	0078h	2	Recommended Multiword DMA transfer cycle time.
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with lORDY flow control
69-79	0000h	20	Reserved
80	0010h	2	Major version number
81	0000h	2	Minor version number
82	7028h	2	Command sets supported
83	5000h	2	Command sets supported
84	4000h	2	Command sets supported
85	0001h	2	Command sets Enable
86	0000h	2	Command sets Enable
87	0002h	2	Command sets Enable
88	001Fh	2	Ultra DMA support and selected
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	0000h	2	Master Password Revision Code
93	600Fh 6F00h 603Fh	2	Hardware reset result (Master) Hardware reset result (Slave) Hardware reset result (Master w/ slave present)
94-127	0000h	68	Reserved
128	0000h	2	Security status
129-159	0000h	64	vendor unique bytes
160	81F4h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0092h	2	CF Advanced True lDE Timing Mode Capability and Setting
164	0000h	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability and Setting 80ns cycle in memory and I/O mode
165-175	0000h	22	Reserved
176-255	0000h	140	Reserved

7.4. ID Table Information (PCMCIA Mode)

Word Address	Default value	Total Bytes	Data Field Type information
0	848Ah	2	General configuration - signature for the PCMCIA-ATA FLASH CARD
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right Justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	XXXXh	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	XXXXh	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0200h	2	Capabilities
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0003h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word57=LSW , Word58=MSW)
59	0100h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0000h	2	Multiword DMA transfer. In PCMCIA mode this value shall be oh
64	0003h	2	Advanced PIO modes supported

Word Address	Default value	Total Bytes	Data Field Type information
65	0000h	2	Minimum Multiword DMA transfer cycle time per word. ln PCMCIA mode this value shall be 0h
66	0000h	2	Recommended Multiword DMA transfer cycle time. In PCMCIA mode this value shall be oh
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with lORDY flow control
69-79	0000h	20	Reserved
80	0000h	2	Major version number
81	0000h	2	Minor version number
82	7028h	2	Command sets supported 0
83	500Ch	2	Command sets supported 1
84	4000h	2	Command sets supported 2
85	0001h	2	Command sets Enable 0
86	0000h	2	Command sets Enable 1
87	0000h	2	Command sets Enable 2
88	0000h	2	Ultra DMA supported and selected
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
93-127	0000h	70	Reserved
128	0000h	2	Security status
129-159	0000h	64	vendor unique bytes
160	81F4h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0000h	2	CF Advanced True lDE Timing Mode Capability and Setting
164	891Bh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability and Setting
165-175	0000h	22	Reserved
176-255	0000h	140	Reserved

Identify Drive Information Description

Word 0: General Configuration

This field indicates that the device is a PCMCIA-ATA Flash Card Storage Card. Note to host implementers: If Word 0 of the Identify drive information is 848Ah then the device complies with the CFA specification, not with the ATA-4 specification.

Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

Words 7-8: Number of Sectors per Card

This field contains the number of sectors per PCMCIA-ATA Flash Card Storage Card. This double word value is also the first invalid address in LBA translation mode.

Words 10-19: Serial Number

This field contains the serial number for this PCMCIA-ATA Flash Card Storage Card and is right justified and padded with spaces (20h).

Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands. This value shall be set to 0004h.

Words 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

Words 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

Word 47: Read/Write Multiple Sector Count

Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h. Bits 7-0 of this word define the maximum number of sectors per block that the PCMCIA-ATA Flash Card Storage Card supports for Read/Write Multiple commands.

Word 49: Capabilities

Bit 13: Standby Timer If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command If bit 13 is set to 0 then the Standby timer operation is defined by the vendor. Bit 11: IORDY Supported If bit 11 is set to 1 then this PCMCIA-ATA Flash Card Storage Card supports IORDY operation. If bit 11 is set to 0 then this PCMCIA-ATA Flash Card Storage Card may support IORDY operation. Bit 10: IORDY may be disabled Bit 10 shall be set to 0, indicating that IORDY may not be disabled. Bit 9: LBA supported Bit 9 shall be set to 1, indicating that this PCMCIA-ATA Flash Card Storage Card supports LBA mode addressing. CF devices shall support LBA addressing. Bit 8: DMA Supported If bit 8 is set to 1 then Read DMA and Write DMA commands are supported. Bit 8 shall be set to 0. Read/Write DMA commands are not currently permitted on CF cards.

Word 51: PIO Data Transfer Cycle Timing Mode

The PIO transfer timing for each PCMCIA-ATA Flash Card Storage Card falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.

Word 53: Translation Parameters Valid

Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any PCMCIA-ATA Flash Card Storage Card that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

Words 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Words 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting

Bits 15-9 are reserved and shall be set to 0. Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid. Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands.

Words 60-61: Total Sectors Addressable in LBA Mode

This field contains the total number of user addressable sectors for the PCMCIA-ATA Flash Card Storage Card in LBA mode only.

Word 64: Advanced PIO transfer modes supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the PCMCIA-ATA Flash Card Storage Card to indicate the advanced PIO modes it is capable of supporting. Of these bits, bits 7 through 2 are reserved for future advanced PIO modes. Bit 0, if set to one, indicates that the PCMCIA-ATA Flash Card Storage Card supports PIO mode 3. Bit 1, if set to one, indicates that the PCMCIA-ATA Flash Card Storage Card supports PIO mode 4.

Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the PCMCIA-ATA Flash Card Storage Card guarantees data integrity during the transfer without utilization of flow control. If this field is supported, Bit 1 of word 53 shall be set to one. Any PCMCIA-ATA Flash Card Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68. If bit 1 of word 53 is set to one because a PCMCIA-ATA Flash Card Storage Card supports a field in words 64-70 other than this field and the PCMCIA-ATA Flash Card Storage Card does not support this field, the PCMCIA-ATA Flash Card Storage Card shall return a value of zero in this field.

Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the PCMCIA-ATA Flash Card Storage Card supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. Any PCMCIA-ATA Flash Card Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the PCMCIA-ATA Flash Card Storage Card. If bit 1 of word 53 is set to one because a PCMCIA-ATA Flash Card Storage Card supports a field in words 64-70 other than this field and the PCMCIA-ATA Flash Card Storage Card does not support this field, the PCMCIA-ATA Flash Card Storage Card shall return a value of zero in this field.

Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by PCMCIA-ATA Flash Card Storage Cards prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers. Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported. If bit 1 of word 82 is set to one, the Security Mode feature set is supported. Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported. Bit 3 of word 82 shall be set to one; the Power Management feature set is supported. Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported. If bit 5 of word 82 is set to one, write cache is supported. If bit 6 of word 82 is set to one, look-ahead is supported. Bit 7 of word 82 shall be set to zero; release interrupt is not supported. Bit 8 of word 82 shall be set to zero; Service interrupt is not supported. Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported. Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported. Bit 11 of word 82 is obsolete. Bit 12 of word 82 shall be set to one; the PCMCIA-ATA Flash Card Storage Card supports the Write Buffer command. Bit 13 of word 82 shall be set to one; the PCMCIA-ATA Flash Card Storage Card supports the Read Buffer command. Bit 14 of word 82 shall be set to one; the PCMCIA-ATA Flash Card Storage Card supports the NOP command.

Bit 15 of word 82 is obsolete. Bit 0 of word 83 shall be set to zero; the PCMCIA-ATA Flash Card Storage Card does not support the Download Microcode command. Bit 1 of word 83 shall be set to zero; the PCMCIA-ATA Flash Card Storage Card does not support the Read DMA Queued and Write DMA Queued commands. Bit 2 of word 83 shall be set to one; the PCMCIA-ATA Flash Card Storage Card supports the CFA feature set. If bit 3 of word 83 is set to one, the PCMCIA-ATA Flash Card Storage Card supports the Advanced Power Management feature set. Bit 4 of word 83 shall be set to zero; the PCMCIA-ATA Flash Card Storage Card does not support the Removable Media Status feature set.

Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by PCMCIA-ATA Flash Card Storage Cards prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers. Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled. If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command. Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported. Bit 3 of word 85 shall be set to one; the Power Management feature set is supported. Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled. If bit 5 of word 85 is set to one, write cache is enabled. If bit 6 of word 85 is set to one, look-ahead is enabled. Bit 7 of word 85 shall be set to zero; release interrupt is not enabled. Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled. Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported. Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported. Bit 11 of word 85 is obsolete. Bit 12 of word 85 shall be set to one; the PCMCIA-ATA Flash Card Storage Card supports the Write Buffer command. Bit 13 of word 85 shall be set to one; the PCMCIA-ATA Flash Card Storage Card supports the Read Buffer command. Bit 14 of word 85 shall be set to one; the PCMCIA-ATA Flash Card Storage Card supports the NOP command.

Bit 15 of word 85 is obsolete. Bit 0 of word 86 shall be set to zero; the PCMCIA-ATA Flash Card Storage Card does not support the Download Microcode command. Bit 1 of word 86 shall be set to zero; the PCMCIA-ATA Flash Card Storage Card does not support the Read DMA Queued and Write DMA Queued commands. If bit 2 of word 86 shall be set to one, the PCMCIA-ATA Flash Card Storage Card supports the CFA feature set. If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command. Bit 4 of word 86 shall be set to zero; the PCMCIA-ATA Flash Card Storage Card does not support the Removable Media Status feature set.

Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete. This command shall be supported on PCMCIA-ATA Flash Card Storage Cards that support security.

Value Time

0 Value not specified

1-254 (Value * 2) minute

255 >508 minutes

Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete. This command shall be supported on PCMCIA-ATA Flash Card Storage Cards that support security.

Value Time

0 Value not specified

1-254 (Value * 2) minutes

255 >508 minutes

Word 91: Advanced power management level value

Bits 7-0 of word 91 contain the current Advanced Power Management level setting.

Word 128: Security Status

Bit 8: Security Level

If set to 1, indicates that security mode is enabled and the security level is maximum.

If set to 0 and security mode is enabled, indicates that the security level is high.

Bit 5: Enhanced security erase unit feature supported

If set to 1, indicates that the Enhanced security erase unit feature set is supported.

Bit 4: Expire

If set to 1, indicates that the security count has expired and Security Unlock and Security Erase Unit are command aborted until a power-on reset or hard reset.

Bit 3: Freeze

If set to 1, indicates that the security is Frozen.

Bit 2: Lock

If set to 1, indicates that the security is locked.

Bit 1: Enable/Disable

If set to 1, indicates that the security is enabled.

If set to 0, indicates that the security is disabled.

Bit 0: Capability If set to 1, indicates that PCMCIA-ATA Flash Card Storage Card supports security mode feature set. If set to 0, indicates that PCMCIA-ATA Flash Card Storage Card does not support security mode feature set.

Word 160: Power Requirement Description

This word is required for PCMCIA-ATA Flash Card Storage Cards that support power mode 1.

Bit 15: VLD

If set to 1, indicates that this word contains a valid power requirement description.

If set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV

This bit is reserved and must be 0.

Bit 13: -XP

If set to 1, indicates that the PCMCIA-ATA Flash Card Storage Card does not have Power Level 1 commands.

If set to 0, indicates that the PCMCIA-ATA Flash Card Storage Card has Power Level 1 commands

Bit 12: -XE

If set to 1, indicates that Power Level 1 commands are disabled.

If set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current

this field contains the PCMCIA-ATA Flash Card Storage Card's maximum current in mA.

Word 162: Key Management Schemes Supported

Bit 0: CPRM support

If set to 1, the device supports CPRM Scheme (Content Protection for Recordable Media)

If set to 0, the device does not support CPRM.

Bits 1-15 are reserved for future additional Key Management schemes.

6. Part number decoder

ATA-68SIX^{8}X^{9}X^{10}X^{11}X^{12} X^{13} X^{14} X^{15} X^{16}

X^{1}X^{2}X^{3}	X^{4}X^{5}	X^{6}X^{7}	X^{8} X^{9} X^{10} X^{11} X^{12}	X^{13}	X^{14}	X^{15}	
ATA	68	SI	128MB 256MB 512MB 001GB 002GB 004GB 008GB 016GB 032GB	C I	F R A	U P M A	

X^{13}	**C :**Standard (0ºC ~ +70ºC) **I:** Industrial (-40ºC ~ +85ºC)
X ^{14}	**F :** Fixed mode **R:** Removable mode **A:** Auto Detect mode
X ^{15}	**U :** UDMA mode **R:** PIO mode **M:** MDMA mode **A:** Auto Detect mode