UD info Corp.

Industrial SD Card
SDC-17UH Series
Product DataSheet

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Revision History

Revision	Draft Date	History	Author
1.0	2022/3/9	New release	Golden Lee

Product Overview

- **Capacity**
  - TLC: 32GB up to 1TB
  - pSLC: 32GB up to 512GB
- **Bus Speed Mode**
  - UHS-II (HD312/FD156)
  - Backward compatibility with UHS-I cards
- **Power Consumption**[Note1]
  - **UHS-I mode**
    - Power Up Current < 250uA
    - Standby Current < 1mA
    - Read Current < 400mA
    - Write Current < 400mA
  - **UHS-II mode**
    - Power Up Current
    - Standby Current
      - Hibernate Mode
      - w/o Hibernate Mode
    - Read Current
  - Write Current
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
- **Supply Voltage 2.7V ~ 3.6V**
  - V_{DD1}: 2.7V ~ 3.6V
  - V_{DD2}: 1.7V ~ 1.95V
- **Temperature Range**
  - Operation: -25°C ~ 85°C
  - Storage: -40°C ~ 85°C
- **Write Protect with mechanical switch**
- **CPRM Optional (Content Protection for Recordable Media)**
- **RoHS Compliant**
- **EMI Compliant**

Notes:

1. Please see Chapter 6.1 Power Consumption for details.

Performance Overview

Capacity	Specification			Flash Configuration			Test Metrix Performance		CrystalDiskMark Win8 (@4000MB)	
	UHS-II	VSC	APP Class	Density	Process	Bit per cell	Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)
32GB	Grade 3	V30	A1	128Gb x2	BiCS3	TLC	275	81	277	80
64GB	Grade 3	V30	A1	256Gb x2	BiCS3	TLC	277	77	281	76
64GB	Grade 3	V60	A1	128Gb x4	BiCS3	TLC	270	154	275	154
128GB	Grade 3	V60	A1	256Gb x4	BiCS3	TLC	268	152	280	154
256GB	Grade 3	V60	A1	256Gb x8	BiCS3	TLC	281	152	278	150
256GB	Grade 3	V60	A1	512Gb x 4	BiCS3	TLC	272	127	276	128
32GB	Grade 3	V90	NA	256Gb x3	BiCS3	pSLC	290	267	284	259
64GB	Grade 3	V90	NA	256Gb x6	BiCS3	pSLC	290	267	286	255
64GB	Grade 3	V90	NA	512Gb x3	BiCS3	pSLC	289	265	285	253
128GB	Grade 3	V90	NA	512Gb x6	BiCS3	pSLC	289	265	286	255
256GB	Grade 3	V90	NA	512Gb x12	BiCS3	pSLC	289	265	287	262
64GB	Grade 3	V60	A1	256Gb x2	BiCS4	TLC	280	100	260	100
128GB	Grade 3	V60	A1	256Gb x4	BiCS4	TLC	280	180	260	100
128GB	Grade 3	V60	A1	512Gb x2	BiCS4	TLC	280	90	260	90
256GB	Grade 3	V60	A1	512Gb x4	BiCS4	TLC	280	180	260	100
32GB	Grade 3	V90	NA	256Gb x3	BiCS4	pSLC	290	269	286	264
64GB	Grade 3	V90	NA	512Gb x3	BiCS4	pSLC	290	269	287	257
128GB	Grade 3	V90	NA	512Gb x6	BiCS4	pSLC	290	269	284	257
256GB	Grade 3	V90	NA	512Gb x12	BiCS4	pSLC	290	269	283	263
64GB	Grade 3	V30	A1	512Gb x1	BiCS5	TLC	190	52	286	53
128GB	Grade 3	V60	A1	512Gb x2	BiCS5	TLC	287	103	286	105
256GB	Grade 3	V60	A1	512Gb x4	BiCS5	TLC	285	195	285	195
256GB	Grade 3	V60	A1	1Tb x2	BiCS5	TLC	287	78	284	78
512GB	Grade 3	V60	A1	1Tb x4	BiCS5	TLC	286	155	280	155
1TB	Grade 3	V60	A1	1Tb x8	BiCS5	TLC				
32GB	Grade 3	V90	NA	512Gb x2	BiCS5	pSLC	288	253	287	259
64GB	Grade 3	V90	NA	512Gb x3	BiCS5	pSLC	290	257	287	261
128GB	Grade 3	V90	NA	1Tb x3	BiCS5	pSLC	290	256	287	261
256GB	Grade 3	V90	NA	1Tb x6	BiCS5	pSLC	290	255	284	256
512GB	Grade 3	V90	NA	1Tb x12	BiCS5	pSLC	290	252	284	254

1. INTRODUCTION

1.1. General Description

The Secure Digital (SD) card is fully compliant with the standards released by the SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver6.10 Final] definitions. Card capacities of the nonsecure area and secure area (if needed) support [Part 3 Security Specification Ver7.0] Specifications.

The UHS-II SD card comes with a 17-pin interface, designed to operate at a maximum throughput (logical/ideal performance) to 312MB/s. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with reasonable power consumption and supports the latest process NAND Flash. UDinfo UHS-II SD Card capacity is from 32GB to 1TB(SDXC).

UHS-II (Ultra High Speed-II) is a new interface and design SD card for 8K and 4K2K recorders, and it is also the most slim and light storage device with more than 245MB/s speed. We can expect more and more hosts and card readers are supporting UHS-II protocol and let removable storage device with high speed transmission securely be highly possible.

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - TLC: 32GB up to 1TB
  - pSLC: 32GB up to 512GB
- **Compliant Specifications - SD Memory Card Specifications:**
  - Compliant with Part 1 Physical Layer Specification Ver. 6.10
  - Compliant with Part 2 File System Specification Ver. 3.00
  - Compliant with Part 3 Security Specification Ver. 7.00
  - Standard Size SD Card Mechanical Addendum Ver. 7.0
- **Support 8K, 4K2K and UltraHD recorder application**
- **Support SD SPI mode**
- **Bus Speed Mode (use 4 parallel data lines)**
  - **Non-UHS mode**
    - Default speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5 MB/sec
    - High speed mode: 3.3V signaling, frequency up to 50MHz, up to 25 MB/sec
  - **UHS mode**
    - SDR12: SDR up to 25MHz, 1.8V signaling
    - SDR25: SDR up to 50MHz, 1.8V signaling
    - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
    - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104 MB/sec
    - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec
  - **UHS-Interface Mode**
    - FD156: Full Duplex mode up to 156MB/s at 52MHz in Range B
    - HD312: Half Duplex with 2 Lanes mode up to 312MB/s at 52MHz in Range B

  Note:

  1. Timing in 1.8V signaling is different from that of 3.3V signaling.
  2. To properly run the UHS mode, please ensure the device supports UHS-I mode.
- **Copyrights Protection Mechanism**
  - Compliant with Part 1 Physical Layer Specification ver. 6.10, CPRM is Optional in SDHC/SDXC.

- **Support Hot Plug**
  - Card removal during read operation will never harm the content
- **Password Protection of cards (optional)**
- **Designed for read intensive and write intensive cards**
- **Built-in write protection features (permanent and temporary)**
- **Write Protect feature using mechanical switch (Full SD Card only)**
- **Electrostatic Discharge (ESD)**
  - ESD protection in pads (contact discharge).
  - ESD protection in non-contact pad area (air discharge).
- **Operation voltage range:**
  - V_{DD1}: 2.7V ~ 3.6V
  - V_{DD2}: 1.7V ~ 1.95V
- **Temperature Range**
  - Operation Temp. Range: -25℃~85℃
  - Storage Temp. Range: -40℃~85℃

3. ELECTRICAL INTERFACE OUTLINE

3.1. Pins Assignment and Descriptions

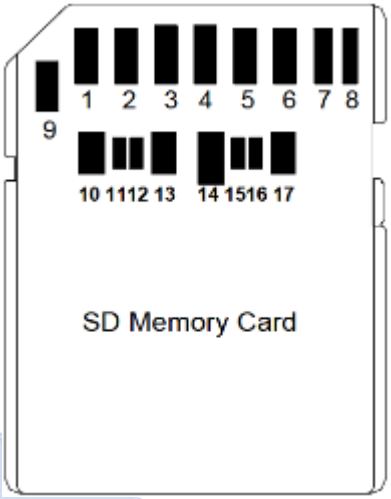


Table 3-1 Standard Size UHS-II Card Pad Assignment

Pin	SD Mode			UHS-II Mode		
	Name	Type[1]	Description	Name	Type	Description
1	CD/DAT3[(2)]	I/O/PP[(3)]	Card Detect/ Data Line[bit3]	-	-	Not Used
2	CMD	PP	Command/Response	-	-	Not Used
3	VSS1	S	Supply voltage ground	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD1	S	Supply voltage (3.3V)
5	CLK	I	Clock	-	-	Not Used
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	RCLK+	I	
8	DAT1	I/O/PP	Data Line[bit1]	RCLK-	I	
9	DAT2	I/O/PP	Data Line[bit2]	-	-	
10				VSS3	S	Supply voltage ground
11				D0+	LVDS	-
12				D0-	LVDS	-
13				VSS4	S	Supply voltage ground
14				VDD2	S	Supply voltage (1.8V)
15				D1-	LVDS	-
16				D1+	LVDS	-
17				VSS5	S	Supply voltage ground

Table 3-2 UHS-II Interface Pad Assignment

Pin	UHS-II Interface		
	Name	Type	Description
4	VDD1	Supply voltage	2.7V to 3.6V
7	RCLK+	Differential Signaling: Input	Clock Input
8	RCLK-	Differential Signaling: Input	Clock Input
10	VSS3	Ground	
11	D0+	Differential Signaling: Input (FD) / Bidirectional (HD)	Input in default
12	D0-	Differential Signaling: Input (FD) / Bidirectional (HD)	Input in default
13	VSS4	Ground	
14	VDD2	Supply Voltage 2	1.7V to 1.95V
15	D1-	Differential Signaling: Output (FD) / Bidirectional (HD)	Output in default
16	D1+	Differential Signaling: Output (FD) / Bidirectional (HD)	Output in default
17	VSS5	Ground	

(1) S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers

(2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer period, with SET_CLR_CARD_DETECT (ACMD42) command.

3.2. SD Bus Topology

The microSD card supports 2 alternative communication protocols, SD and SPI BUS mode.

Host can choose either one of both bus mode, same data can be read or written by both modes.

SD mode allows 4-bits data transfer way, it provides high performance. SPI mode supports 1-bit data transfer and of course the performance is lower compared to SD mode.

3.3. SD Bus Mode Protocol

In default speed, the SD Memory Card bus has a single master (application); multiple slaves (Cards), synchronous star topology (refer to Figure 3-2). In high speed and UHS-I, the SD Memory Card bus has a single

master (application) and single slave (card), synchronous point to point topology. Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0-DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.

During initialization process commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simply the handling of the card stack, after the initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet. SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Memory Card will use only DAT0 for data transfer. After initialization the host can change the bus width (number of data active lines). This feature allows easy tradeoff between HW cost and system performance. Note that while DAT1 to DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode). For SDIO cards DAT1 and DAT2 are used for signaling.

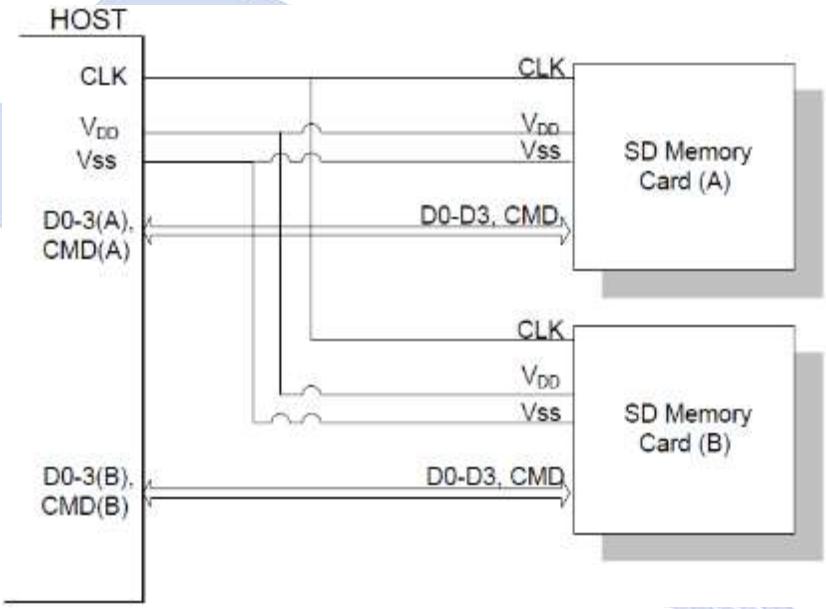


Figure 3-1 SD Memory Card System Bus Topology

The SD bus includes the following signals:

CLK: Host to card clock signal

CMD: Bidirectional Command/Response signal

DAT0-DAT3: 4 Bidirectional data signals

VDD, Vss1, Vss2: Power and ground signals

Table 3-3 SD Mode Command Set

Card Command Class (CCC)	0	1	2	3	4	5	6	7	8	9	10	11
	Basic	Command Queue	Block read	Reserved	Block Write	Erase	Write Protect-ion	Lock Card	Application Specific	I/O mode	Switch	Extension
CMD0	+											
CMD2	+											
CMD3	+											
CMD4	+											
CMD5										+		
CMD6											+	
CMD7	+											
CMD8	+											
CMD9	+											
CMD10	+											
CMD11	+											
CMD12	+											
CMD13	+											
CMD15	+											
CMD16			+		+			+				
CMD17			+									
CMD18			+									
CMD19			+									
CMD20			+		+							
CMD21												+
CMD23			+		+							
CMD24					+							
CMD25					+							
CMD27					+							
CMD28							+					
CMD29							+					
CMD30							+					
CMD32						+						
CMD33						+						
CMD34											+	
CMD35											+	
CMD36											+	
CMD37											+	
CMD38						+						
CMD40								+				

Card Command Class (CCC)	0	1	2	3	4	5	6	7	8	9	10	11
	Basic	Command Queue	Block read	Reserved	Block Write	Erase	Write Protect-ion	Lock Card	Application Specific	I/O mode	Switch	Extension
CMD42								+				
CMD43		+										
CMD44		+										
CMD45		+										
CMD46		+										
CMD47		+										
CMD48												+
CMD49												+
CMD50											+	
CMD52										+		
CMD53										+		
CMD55									+			
CMD56									+			
CMD57											+	
CMD58												+
CMD59												+
ACMD6									+			
ACMD13									+			
ACMD14									+			
ACMD15									+			
ACMD16									+			
ACMD22									+			
ACMD23									+			
ACMD28									+			
ACMD41									+			
ACMD42									+			
ACMD51									+			

Commands	Support Requirements
CMD0	Mandatory
CMD2	Mandatory
CMD3	Mandatory
CMD4	Mandatory
CMD5	Optional
CMD6	Mandatory for cards version 1.10 and after
CMD7	Mandatory
CMD8	Mandatory for cards version 2.00 and after
CMD9	Mandatory
CMD10	Mandatory
CMD11	Mandatory for cards supporting UHS-I. Optional for cards that do not support UHS-I.
CMD12	Mandatory
CMD13	Mandatory
CMD15	Mandatory
CMD16	Mandatory
CMD17	Mandatory
CMD18	Mandatory
CMD19	Mandatory for cards supporting UHS-I. Optional for cards that do not support UHS-I.
CMD20	Not supported for SDSC cards. Mandatory for SDHC and SDXC cards that support Video Speed Class. Optional for SDHC cards that support: a.) Speed Class; or b.) UHS Speed Grade, and do not support Video Speed Class Mandatory for SDXC cards that support Speed Class or UHS Speed Grade.
CMD21	Optional
CMD23	Not supported for SDSC cards. Mandatory for SDHC and SDXC cards that support UHS104. Optional for SDHC and SDXC cards that do not support UHS104.
CMD24	Mandatory for writable types of cards
CMD25	Mandatory for writable types of cards
CMD27	Mandatory for writable types of cards
CMD28	Optional
CMD29	Optional

Commands	Support Requirements
CMD30	Optional
CMD32	Mandatory for writable types of cards
CMD33	Mandatory for writable types of cards
CMD34 - 37	Optional for cards version 1.10 and after
CMD38	Mandatory for writable types of cards Discard and FULE supports optional
CMD40	Optional
CMD42	Optional for cards version 1.01 and 1.10 Mandatory for cards version 2.00 and after COP support is optional for CMD42
CMD43 - 47	Mandatory for cards supporting Command Queue
CMD48	Optional Mandatory for cards supporting Performance Enhancement functions (refer to 5.8.2)
CMD49	Optional Mandatory for cards supporting Performance Enhancement functions (refer to 5.8.2)
CMD50	Optional for cards version 1.10 and after
CMD52	Optional
CMD53	Optional
CMD55	Mandatory
CMD56	Mandatory
CMD57	Optional for cards version 1.10 and after
CMD58	Optional
CMD59	Optional
ACMD6	Mandatory
ACMD13	Mandatory
ACMD14	Optional
ACMD15	Optional
ACMD16	Optional
ACMD22	Mandatory for writable types of cards
ACMD23	Mandatory for writable types of cards
ACMD28	Optional
ACMD41	Mandatory
ACMD42	Mandatory
ACMD51	Mandatory

3.4. SPI Bus Mode Protocol

While the SD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel by byte oriented. Every command or data block is built for 8-bit bytes and is byte aligned with the CS signal (i.e. the length is a multiple of 8 clock cycles). The card starts to count SPI bus clock cycle at the assertion of the CS signal. Every command or data token shall be aligned with 8-clock cycle boundary.

Similar to the SD Memory Card Protocol, the SPI messages consist of command, response and data-block tokens.

The advantage of SPI mode is reducing the host design effort, especially for MMC host side, it just be modified by little change. Note: please use SD card specification to implement SPI mode function, not use MMC specification. For example, SPI mode is initialized by ACMD41, and the registers are different from MMC card, especially CSD register.

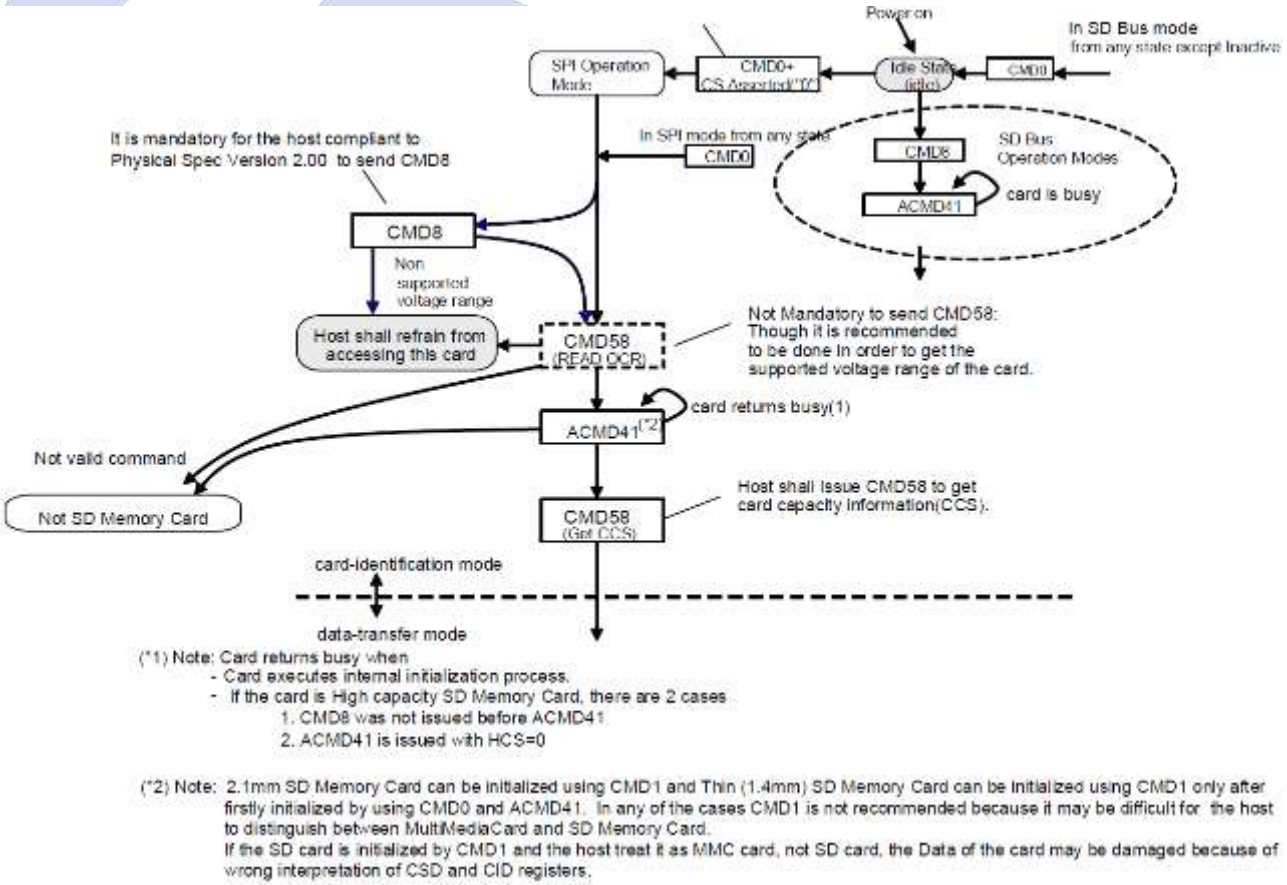


Figure 3-2 SD Memory Card State Diagram (SPI mode)

Table 3-4 SPI Mode Command Set

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	Class Description	Basic	Reserved	Block read	Reserved	Block Write	Erase	Write Protection	Lock Card	Application Specific	I/O mode	Switch	Reserved
CMD0	Mandatory	+											
CMD1	Mandatory	+											
CMD5	Optional										+		
CMD6[2]	Mandatory											+	
CMD8[3]	Mandatory	+											
CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD24	Mandatory[1]					+							
CMD25	Mandatory[1]					+							
CMD27	Mandatory[1]					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32	Mandatory[1]						+						
CMD33	Mandatory[1]						+						
CMD34	Optional											+	
CMD35	Optional											+	
CMD36	Optional											+	
CMD37[2]	Optional											+	
CMD38	Mandatory[1]						+						
CMD42[4]	(Note 4)								+				
CMD50[2]	Optional											+	
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory									+			
CMD56	Mandatory									+			
CMD57[2]	Optional											+	
CMD58	Mandatory	+											
CMD59	Mandatory	+											

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	**Class Description**	**Basic**	**Reserved**	**Block read**	**Reserved**	**Block Write**	**Erase**	**Write Protection**	**Lock Card**	**Application Specific**	**I/O mode**	**Switch**	**Extension**
ACMD13	Mandatory									+			
ACMD22	Mandatory[1]									+			
ACMD23	Mandatory[1]									+			
ACMD41	Mandatory									+			
ACMD42	Mandatory									+			
ACMD51	Mandatory									+			

Note:

(1) The commands related write and erase are mandatory only for the Writable types of Cards.

(2) This command was defined in spec version 1.10.

(3) This command is newly defined in version 2.00.

(4) This command is optional in version 1.01 and 1.10 and mandatory from version 2.00.
COP support is optional for CMD42.

3.5. SD/microSD card initialization

Figure 3-4 presents the initialization flow chart for UHS-I hosts and Figure 3-5 shows sequence of commands to perform voltage switch.

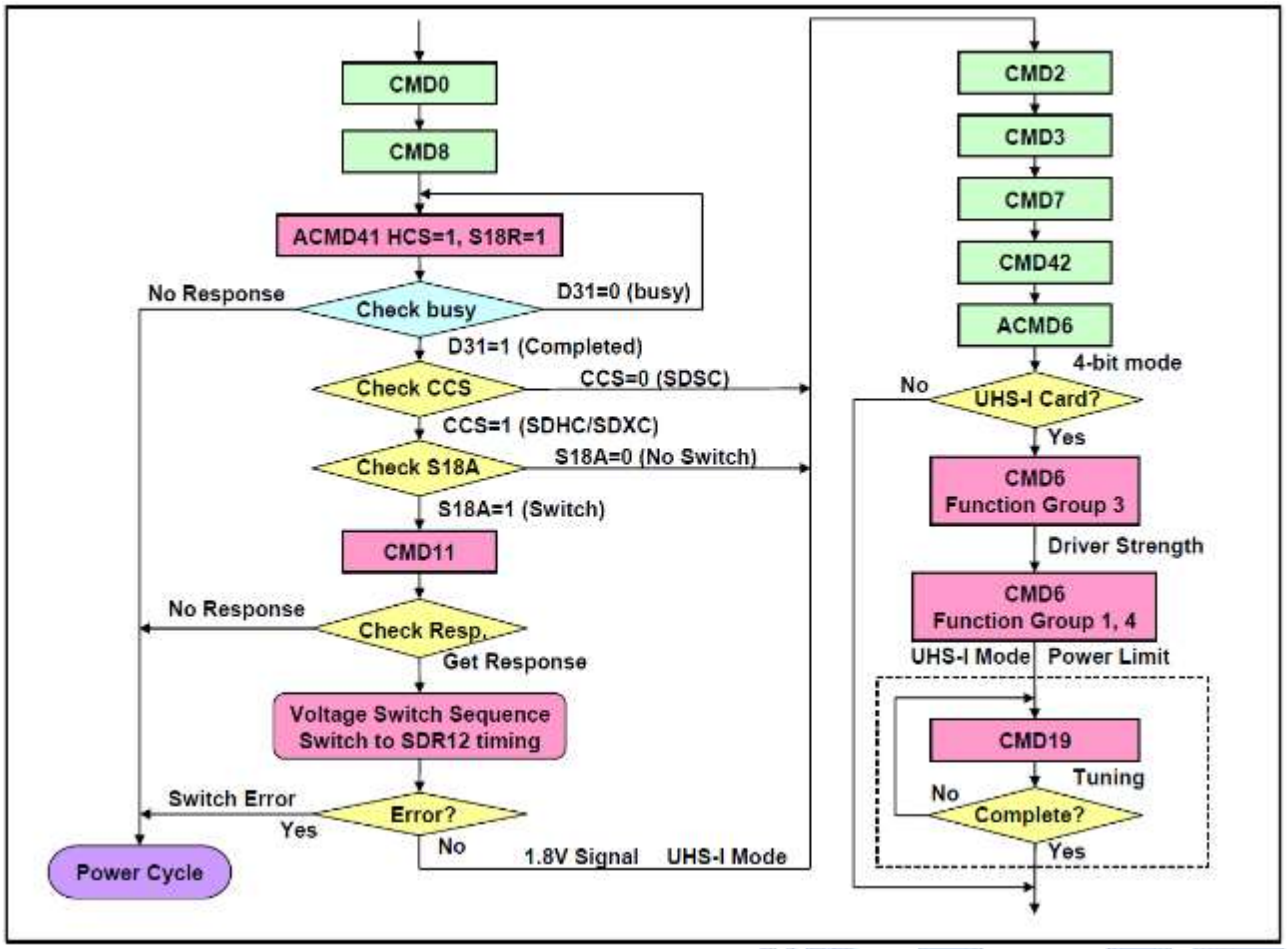


Figure 3-3 UHS-I Host Initialization Flow Chart

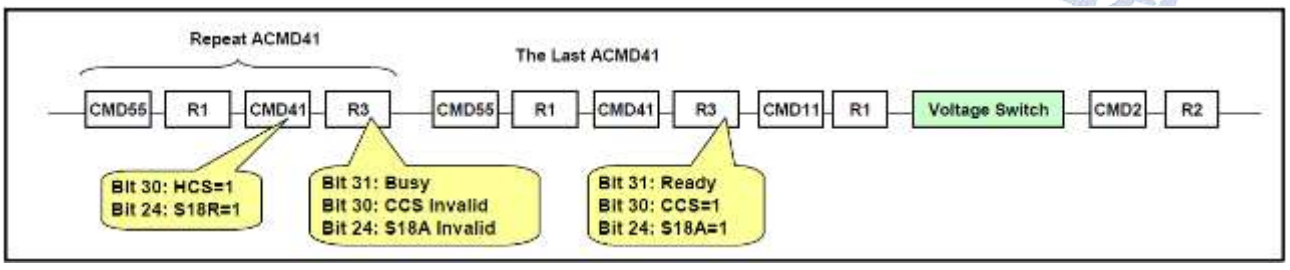


Figure 3-4 ACMD41 Timing Followed by Voltage Switch Sequence

When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument.

If Bit31 indicates ready, host needs to check CCS and S18A.

The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level.

Table 3-5 S18R and S18A Combinations

Current Signaling Level	S18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 18 signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

To change signaling level at the same time between host and card, signal voltage switch sequence is invoked by CMD11 as shown in Figure 3-6. CMD11 is issued only when S18A=1 in the response of ACMD41.

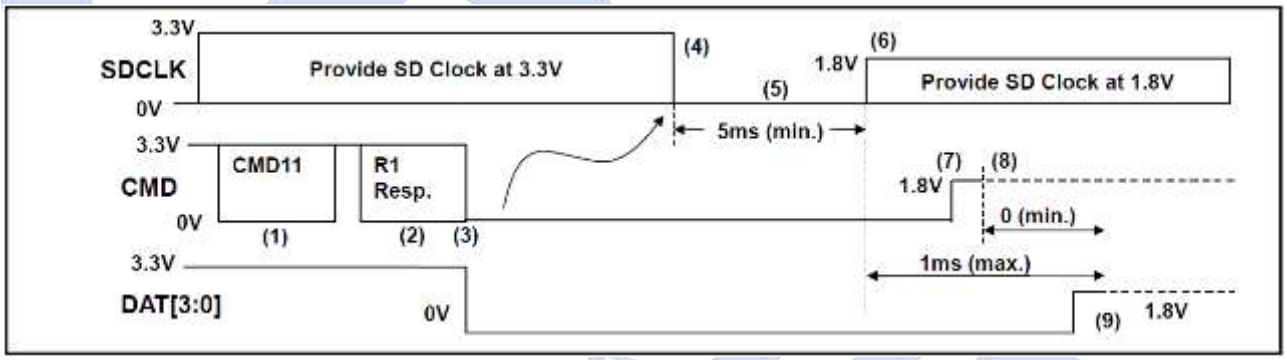


Figure 3-5 Signal Voltage Switch Sequence

4. ENVIRONMENTAL SPECIFICATIONS

4.1. Environmental Conditions

Temperature and Humidity

- Storage Temperature Range
  - -40°C ~ 85°C
- Operation Temperature Range
  - Standard Temperature: -25°C ~ 85°C
  - Wide Temperature: -40°C ~ 85°C (for pSLC)

Table 4-1 High Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	85°C	0% RH	96 hours
Storage	85°C	0% RH	500 hours

Result: No any abnormality is detected.

Table 4-2 Low Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	-25°C	0% RH	96 hours
Storage	-40°C	0% RH	168 hours

Result: No any abnormality is detected.

Table 4-3 High Humidity Test Condition

	Temperature	Humidity	Test Time
Operation	25°C	95% RH	1 hour
Storage	40°C	93% RH	500 hours

Result: No any abnormality is detected.

Durability Test

Table 4-4 Durability Specification

	Mating Cycles
Non UHS-II SD Card Connector	10,000 cycles
UHS-II SD Card with UHS-II SD Card Connector	5,000 cycles
Non UHS-II SD Card with UHS-II SD Card Connector	3,000 cycles

Result: No any abnormality is detected when power on.

Shock

Table 4-5 Shock Specification

	Acceleration Force	Half Sin Pulse Duration
Industrial SD/microSD	500G	0.5ms

Result: No any abnormality is detected when power on.

Vibration

Table 4-6 Vibration Specification

	Condition		Vibration Orientation
	Frequency/Displacement	Frequency/Acceleration	
Industrial SD/microSD	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	X, Y, Z axis/30 min for each

Result: No any abnormality is detected when power on.

Drop

Table 4-7 Drop Specification

	Height of Drop	Number of Drop
Industrial SD/microSD	150cm free fall	6 face; 1 time/face

Result: No any abnormality is detected when power on.

Bending

Table 4-8 Bending Specification

	Force	Action
Industrial SD/microSD	≥ 10N	Hold 1min/5times

Result: No any abnormality is detected when power on.

Switch Cycle Test

Table 4-9 Switch Cycle Test Specification

	Force	Number of Switch Cycle
Industrial SD/microSD	0.4 ~ 0.5N	1,000 cycles

Result: No any abnormality is detected when power on.

Torque

Table 4-10 Torque Specification

	Force	Action
Industrial SD/microSD	0.15N-m or ±2.5 deg	Hold 30 seconds/5times

Result: No any abnormality is detected when power on.

Waterproof Test

Table 4-11 Waterproof Test Specification

	Condition	Action
Industrial SD/microSD	The lowest point of unit is locating 1000mm below surface of the water	Hold 30 minutes in storage state

Result: No any abnormality is detected when power on.

Durability Mating Cycle Test

Table 4-12 Mating Cycle Test Specification

	Number of Mating Cycle
Industrial SD/microSD	10,000 cycles

Result: No any abnormality is detected when power on.

Electrostatic Discharge (ESD)

Table 4-13 ESD Specification

	Condition	Result
Industrial SD/microSD	**Non-operating:** Contact: ±4KV; 5 times/Pin Air: ±15KV; 5 times/Position	PASS
	Operating: Air: ±8KV; 10 times/Position (EN55024-61000-4-2)	B grade PASS

EMI Compliance

- FCC: CISPR22
- CE: EN55032
- BSMI 13438

4.2. MTBF

MTBF, an acronym for Mean Time between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of UDinfo's SD/microSD is more than 2,000,000 hours.

Analysis software: Relex7.3

Analysis Method: Telcordia SR-332, Reliability Prediction of Electronic Equipment.

Operational Temperature(Ta) of test environment: 30℃

Temperature(Tc) of Device when evaluation: 45℃

5. SD CARD COMPARISON

Table 5-1 Comparing SDSC, SDHC, and SDXC

	SD6.10 SDSC	SD6.10 SDHC	SD6.10 SDXC
File System	FAT 12/16	FAT32	exFAT
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.7v – 3.6v (for operation)	Support	Support	Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

Table 5-2 Comparing UHS Speed Grade Symbols

	U1 (UHS Speed Grade 1)	U3 (UHS Speed Grade 3)
Operable Under	*UHS-I Bus I/F, UHS-II Bus I/F	
SD Memory Card	SDHC UHS-I and UHS-II, SDXC UHS-I and UHS-II	
Mark		
Performance	10 MB/s minimum write speed	30 MB/s minimum write speed
Applications	Full higher potential of recording real-time broadcasts and capturing large-size HD videos.	Capable of recording 4K2K video.

*UHS (Ultra High Speed), the fastest performance category available today, defines bus-interface speeds up to 312 Megabytes per second for greater device performance. It is available on SDXC and SDHC memory cards and devices.

Table 5-3 Comparing Video Speed Class Symbols

	V6	V10	V30	V60	V90
Bus Speed Mode Requirement	Non UHS UHS-I UHS-II	Non UHS UHS-I UHS-II	Non UHS UHS-I UHS-II	UHS-II	UHS-II
Card Capacity	SDHC, SDXC				
Mark	V6	V10	V30	V60	V90
Performance (Minimum Sequential Write Speed)	6MB/s	10MB/s	30MB/s	60MB/s	90MB/s
Applications	Standard Video	Full HD Video HD Video	4K2K Video Full HD Video	4K2K Video	8K Video

6. ELECTRICAL SPECIFICATIONS

6.1. Power Consumption

The table below is the power consumption of SD card with different flash memory types.

Table 6-1 Power Consumption of SD card (UHS-I Mode)

Flash Mode		Max. Power Up Current (uA)	Max. Standby Current (uA)	Max. Read Current (mA)	Max. Write Current (mA)
Default Speed Mode		250	1000	150 @3.6V	150[3] @3.6V
High Speed Mode		250	1000	200 @3.6V	200 @3.6V
UHS-I Mode	UHS50/DDR50	250	1000	400 @3.6V	400 @3.6V
	UHS104/DDR50	250	1000	400 @3.6V	400 @3.6V

Note:

1. Power consumptions are measured at room temperature.
2. Power consumption of Max. Standby Current is for SD cards under and including 64GB only. For 128GB and 256GB, the power consumption is to be determined.
3. For SDXC, up to 100mA from VDD1 when XPC=0; up to 150mA from VDD1 when XPC=1.

Table 6-2 SD card RMS Power Consumption (UHS-II Mode)

Bus Speed Mode		Max. Power Up Current (uA)		Max. Standby Current (uA)				Max. Read Current (mA)		Max. Write Current (mA)	
				w/o Hibernate Mode		Hibernate Modec					
		V_{DD1}	V_{DD2}	V_{DD1}	V_{DD2}	V_{DD1}	V_{DD2}	V_{DD1}	V_{DD2}	V_{DD1}	V_{DD2}
UHS-II Mode	FD156	500	200	1380	120	80	120	200	50	200	50
	HD312	500	200	1380	120	80	120	200	50	250	50

Table 6-3 SD card Peak Power Consumption (UHS-II Mode)

Bus Speed Mode		Max. Power Up Current (uA)		Max. Standby Current (uA)				Max. Read Current (mA)		Max. Write Current (mA)	
				w/o Hibernate Mode		Hibernate Modec					
		V_{DD1}	V_{DD2}	V_{DD1}	V_{DD2}	V_{DD1}	V_{DD2}	V_{DD1}	V_{DD2}	V_{DD1}	V_{DD2}
UHS-II Mode	FD156	1000	650	1380	120	80	120	350	50	400	50
	HD312	1000	650	1380	120	80	120	350	50	450	50

Note:

1. Power consumptions are measured at room temperature.
2. Table 6-2 is determined by RMS value and Table 6-3 is determined by peak value. SDA only specify RMS value.

3. Switch to hibernate mode when standby is UDinfo cards' default setting. Card will not enter hibernate mode only if host does not support.
4. Max. write VDD1 current of HD312 mode peak value is over 400mA.

6.2. Working Rating

6.2.1. Absolute Maximum Rating

Item	Symbol	Parameter	Min.	Max.	Unit
1	T_a	Operating Temperature	-25	+85	°C
2	T_{st}	Storage Temperature	-40	+85	°C

Parameter	Symbol	Min.	Max.	Unit
Operating Temperature	T_a	-25	+85	°C
V_{DD} Voltage	V_{DD}	2.7	3.6	V

6.3. DC Characteristic

6.3.1. Bus Operation Conditions for 3.3V Signaling

Table 6-4 Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH}=-2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL}=2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

Table 6-5 Peak Voltage and Leakage Current

Parameter	Symbol	Min.	Max	Unit	Remarks
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 6-6 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.58	V	

Table 6-7 Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min.	Max	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected

6.3.2. Bus Operation Conditions for UHS-II

Table 6-8 Bus Operation Conditions of VDD2

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V_{DD2}	1.7	1.96	V	
Capacitance connected to VDD2	C_{c2}	-	2	uF	

Item	Value				Note
	Min.	Type	Max	Unit	
VDD1 Supply voltage	2.7	3.3	3.6	V	Note 1
VDD2 Supply voltage	1.7	1.8	1.95	V	Note 2

Note 1: VDD1 of 1.8V is under evaluation.

Note 2: VDD2 of 1.2V is optional for embedded Device.

Item	Value				Note
	Min.	Type	Max	Unit	
Leakage current of each UHS-II pin			10	uA	Absolute value. Note 1,2,3

Note 1: Refer to leakage of D0+, D0-, D1+, D1-, RCLK+ and RCLK-.

Note 2: When pin is at input state, with static valid input voltage.

Note 3: Input termination resistor is disconnected.

6.3.3. Bus Signal Line Load

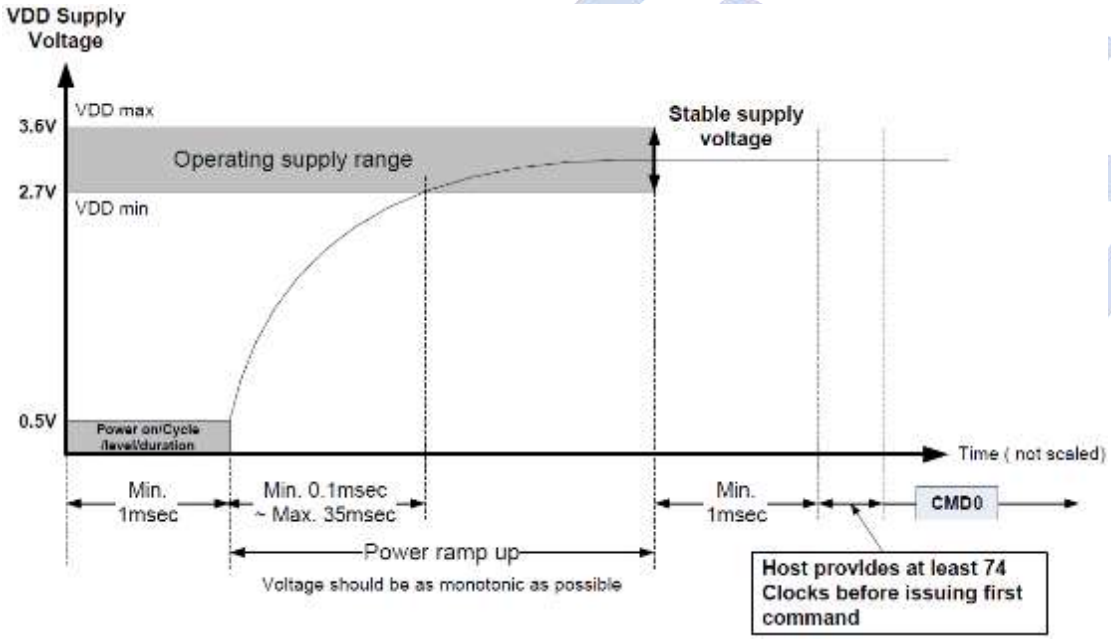
Bus Operation Conditions – Signal Line's Load

Total Bus Capacitance = C_{HOST} + C_{BUS} + N C_{CARD}

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST} + C_{BUS} shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

6.3.4. Power Up Time of UHS-I Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V.

(2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD (min.) and VDD (max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

(4) Host shall wait until VDD is stable.

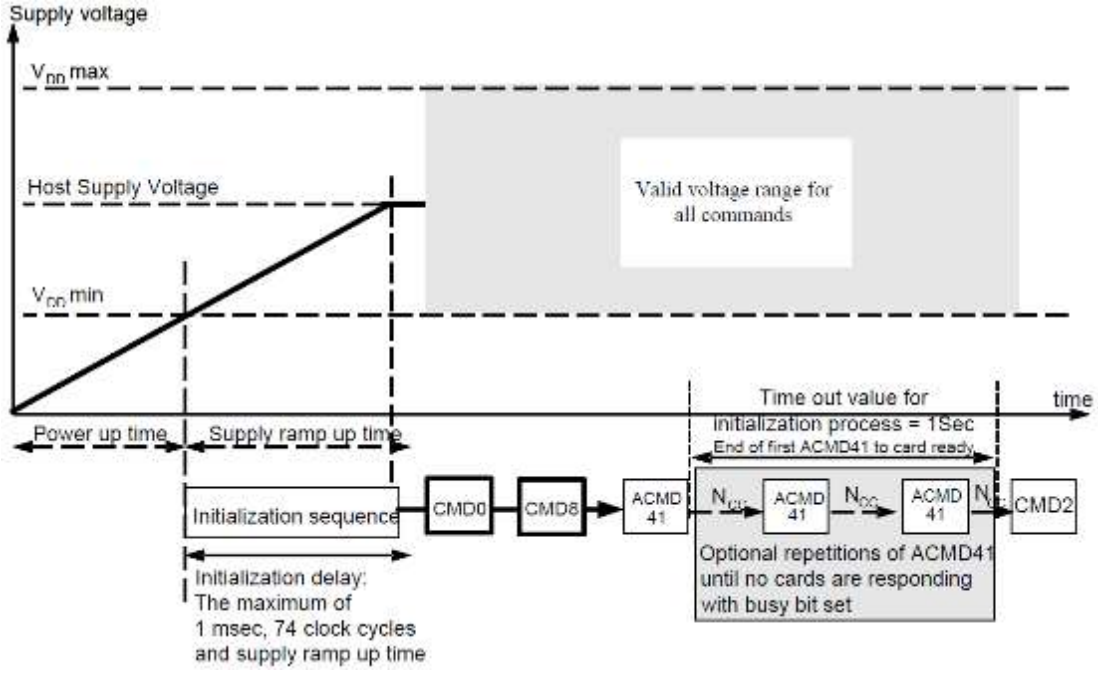
(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

Power Down and Power Cycle

- When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
- If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State*. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

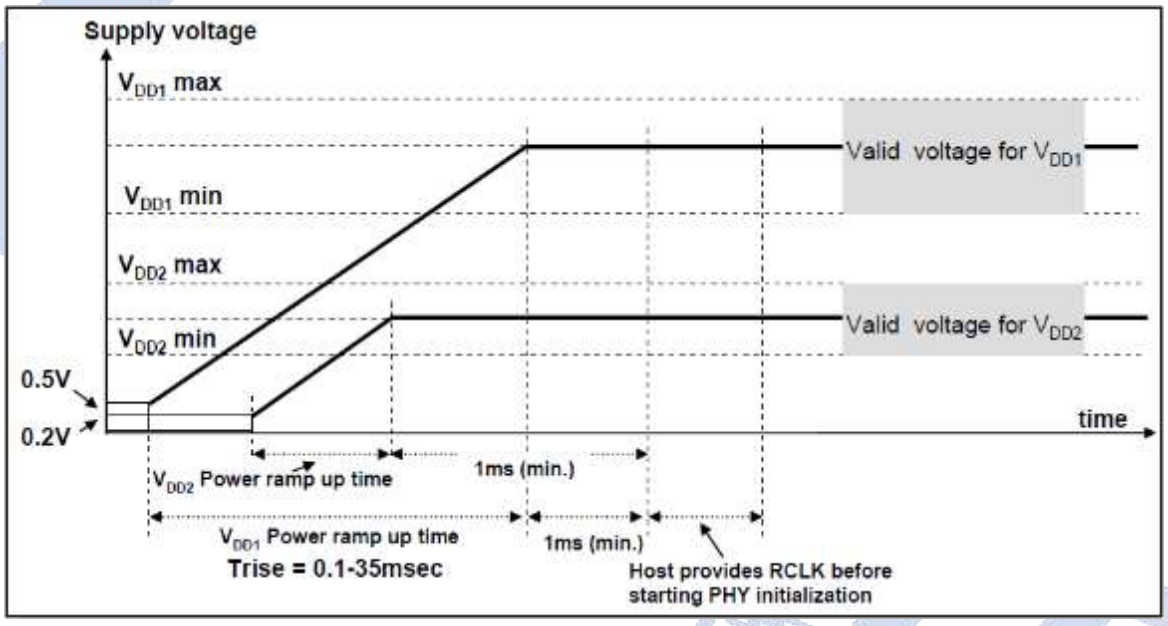
6.3.5. Power Up Time of UHS-I Card

A device shall be ready to accept the first command within 1ms from detecting VDD min. Device may use up to 74 clocks for preparation before receiving the first command.



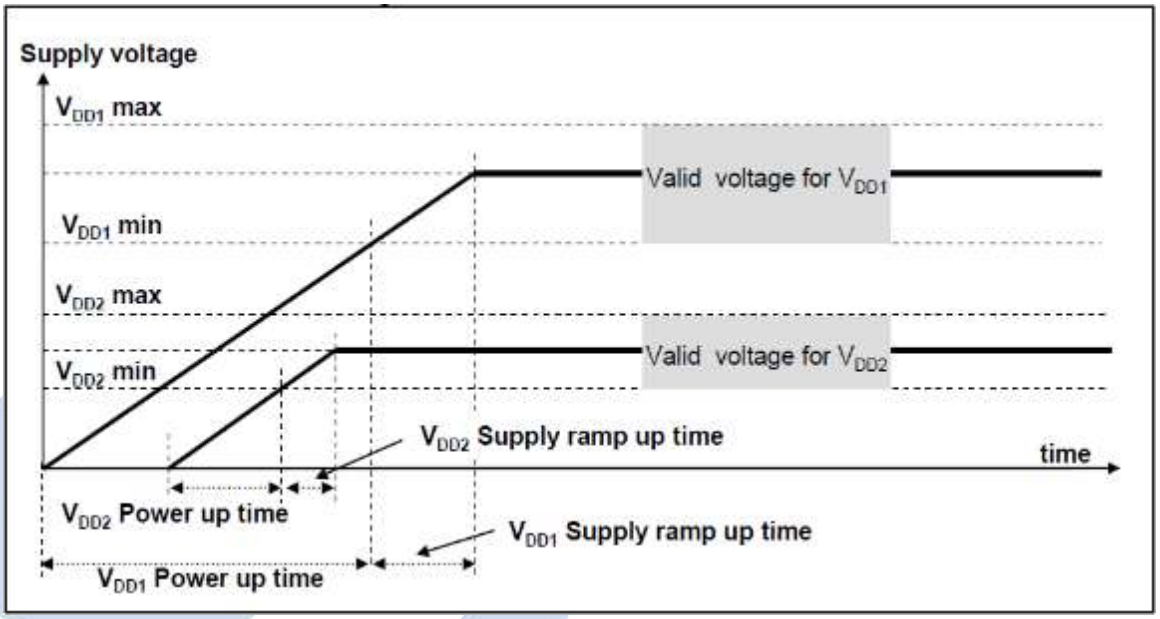
6.3.6. Power Up Sequence of UHS-II Host

- Power up and ramp up of VDD1 and VDD2 should be monotonic.
- Either power up order is allowed for VDD1 and VDD2
- Trise shall be 0.1-35ms.
- Host shall wait until both VDD1 and VDD2 are stable.
- After additional 1ms stable time from both VDD1 and VDD2 are stable, host starts to provide RCLK and then starts PHY Initialization.
- Once VDD2 is supplied, host needs to supply VDD2 until power cycle.
- When power cycle is executed, keep VDD1 less than 0.5V and VDD2 less than 0.2V at least 1ms before starting power up.



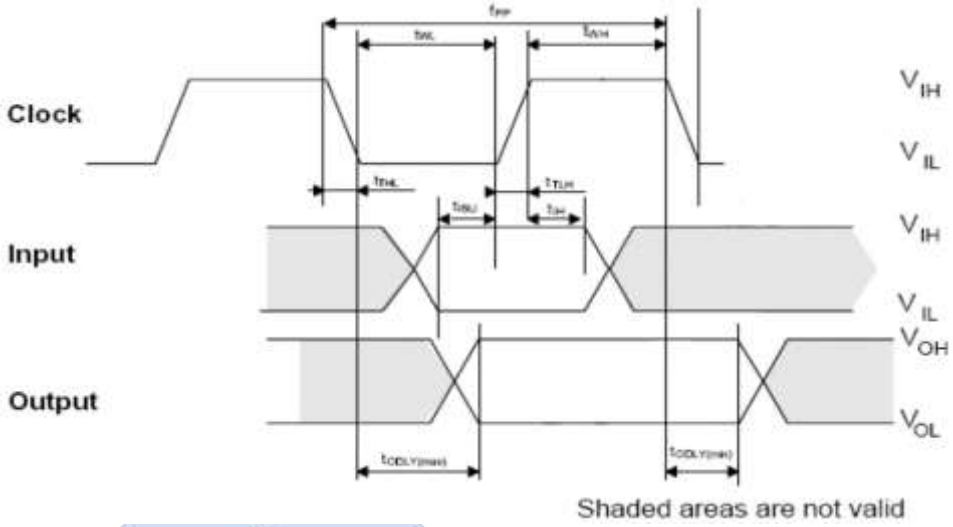
6.3.7. Power Up Sequence of UHS-II Card

Power up order of VDD1 and VDD2 should be expected and card power up is dependent on later one. UHS-II Card shall be ready to start PHY Initialization with 1ms from detecting later of VDD1 min or VDD2 min.



6.4. AC Characteristic

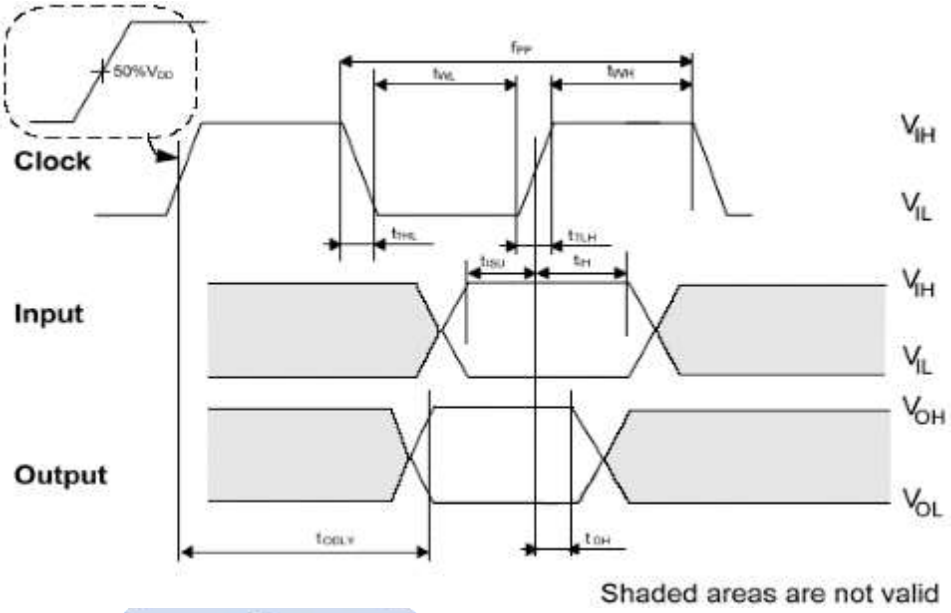
6.4.1. SD Interface Timing (Default)



Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card} ≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0[(1)]/100	400	KHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≤ 40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L ≤ 40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

6.4.2. SD Interface Timing (High-Speed Mode)



Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	CL ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, the host shall drive only one card.

6.4.3. SD Interface Timing (SDR12, SDR25, SDR50 and SDR104 Modes)

Input

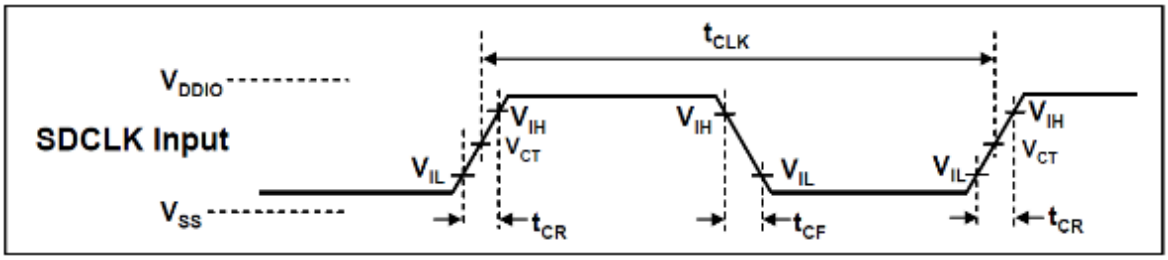
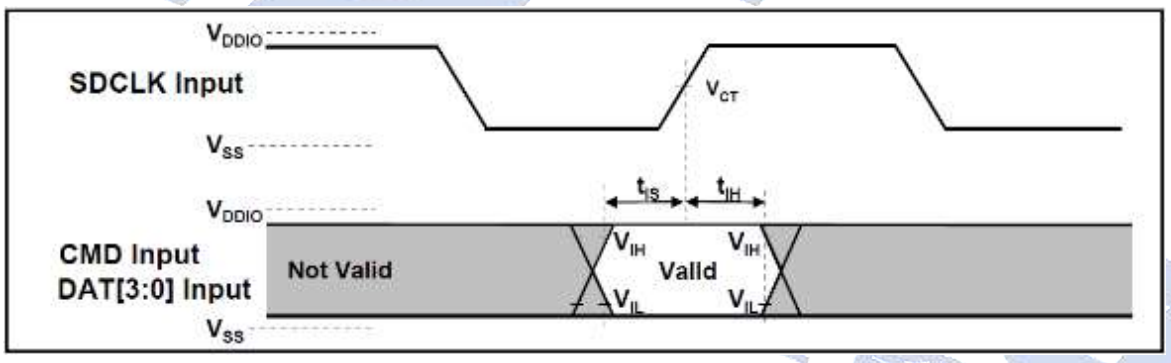


Table 6-9 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, CCARD=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, CCARD=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency
Clock Duty	30	70	%	

- **SDR50 and SDR104 Input Timing:**



Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8	-	ns	C_{CARD} =5pF, V_{CT}= 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} =10pF, V_{CT}= 0.975V
t_{IH}	0.8	-	ns	C_{CARD} =5pF, V_{CT}= 0.975V

Card Input Timing

Output

- **Output (SDR12, SDR25, SDR50 mode):**

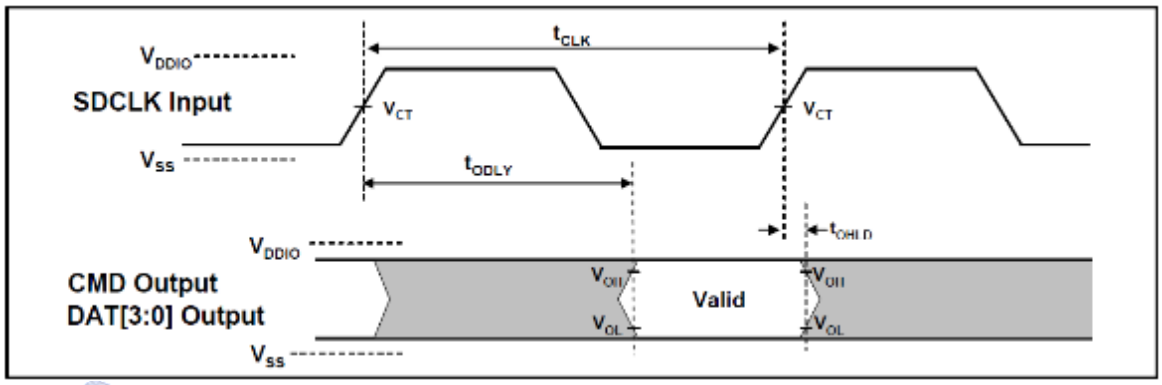


Table 6-10 Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK}>=10.0ns, C_L=30pF, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	t_{CLK}>=20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12,
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L=15pF

- **Output (SDR104 mode):**

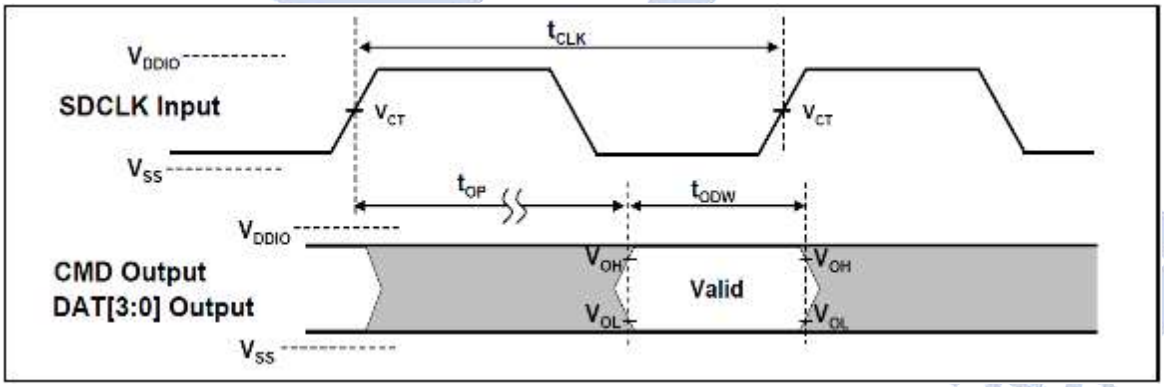
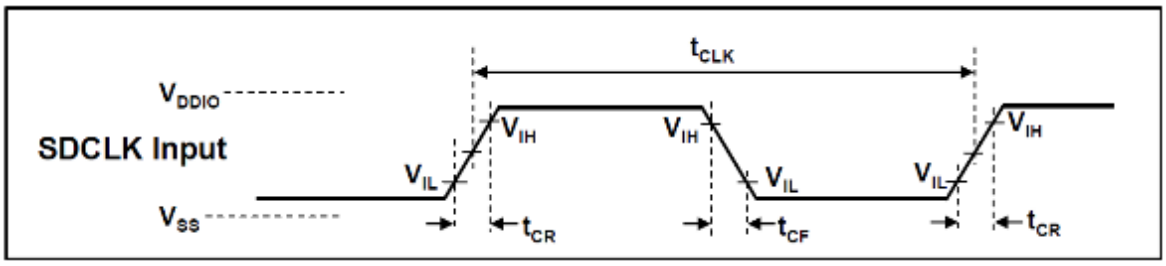


Table 6-11 Output Timing of Variable Window (SDR104)

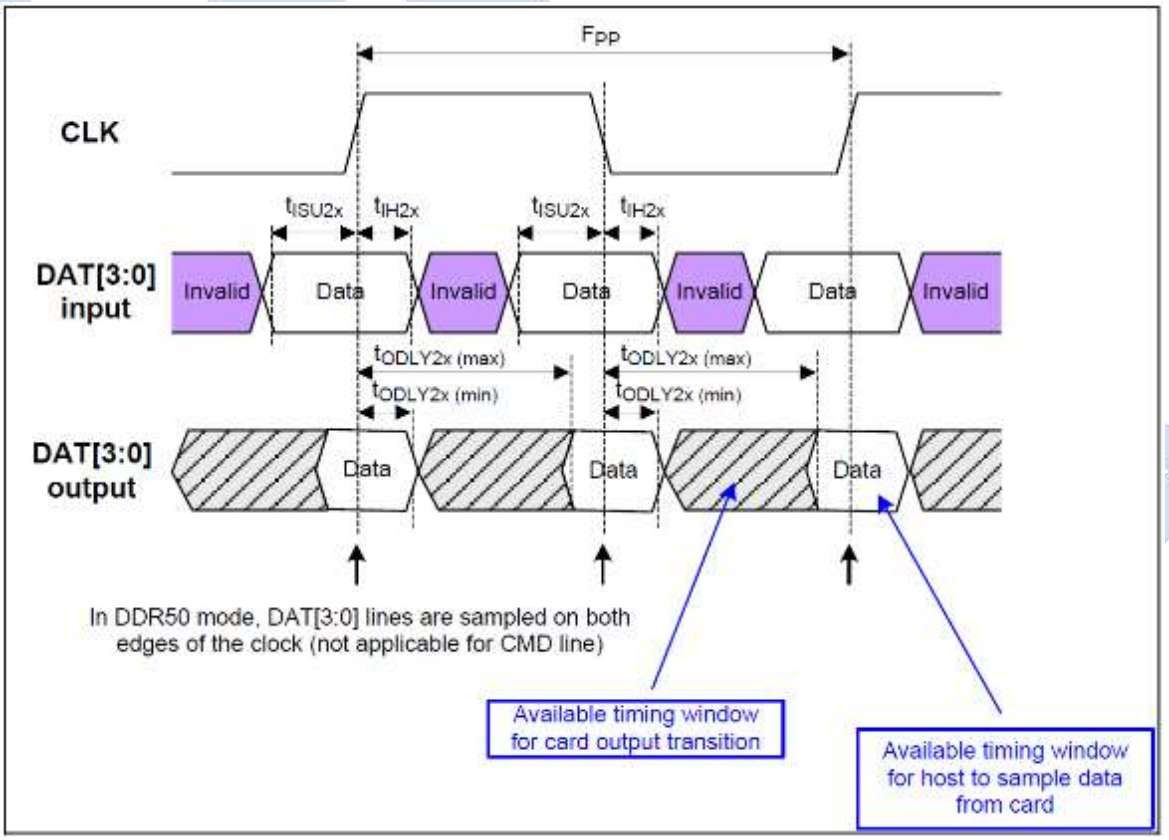
Symbol	Min	Max	Unit	Remark
t_{OP}	-	2	UI	Card Output Phase
$\triangle t_{OP}$	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

6.4.4. SD Interface Timing (DDR50 Modes)



Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2 * t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

Clock Signal Timing



Timing Diagram DAT Inputs/Outputs Reference to CLK in DDR50 mode

Table 6-12 Bus Timing – Parameter Values (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	$C_L \leq 30$ pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25$ pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	$C_L \geq 15$ pF (1 card)

7. HOST SYSTEM DESIGN GUIDELINES

7.1. Efficient Data Writing to SD Memory Card

In order to optimize sequential writing performance and WAF (Write Amplification Factor), it is recommended to use allocation unit (AU) writing.

It is recommended that Multiple_Block_Write shall be used as a command for writing data, and the size of data written by each command should be the FAT cluster x n (n: integer)

7.1.1. Write_Single_Block and Write_Multiple_Block

Write single block (CMD24) was written by one sector (512Bytes), which is suitable to write small area such like updating file system area (FAT). Besides, Write multiple blocks (CMD25) is a command for writing data to blocks that have sequential address per command, which is suitable to write large area such as user data. Write multiple blocks with a cluster unit (512Byte x 128 Sectors = 64KByte) in the file system is an efficient access to the flash memory, it is obviously to provide higher speed to compared to single write block.

And it could be estimated that SD card internal process would be reduced to save power consumption and flash write amplification factor, that is why the efficient data writing was recommended. To avoid the command issued by 512Bytes with single write block, software processes in the host device become faster. For this operation, check the sectors in the SD card and file system as Figure 7-1

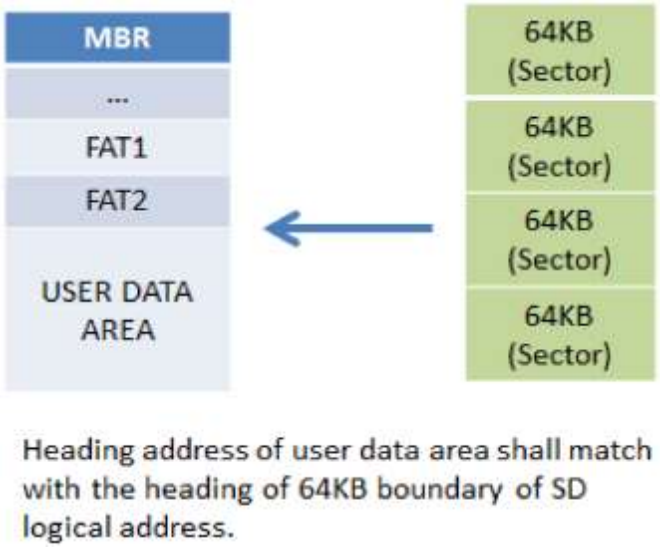


Figure 7-1 Matching between logical address and file system

Note: Large Cluster unit is better for performance and WAF, for example, 128KB, 256KB or 512KB. Large cluster unit also can save write command numbers and few transfer time.

7.2. Basic Process of Error Handling

7.2.1. Retry Process

Execute the process by sending commands again, especially for signal issue between card and host.

7.2.2. Recovery Process

Confirm card status is in Transfer State, if card status is not in Transfer State, please issue Stop command to recover it and execute or continue flow. If there was UECC during read/write status, we could use recovery process to recover it.

7.2.3. Tuning Write Command Process

In order to adjust Host CMD and CLK timing, the way is issue tuning command to confirm what the device response and data was received by host. Based on the response, host was adjusting the timing step by step and recording the pass range. Through this flow host could adjust the appropriate timing settings to avoid unexpected handshaking issue.

7.2.4. Tuning Read Command Process

In order to adjust Host CLK and DAT timing, the way is issue tuning command to confirm what the device response and data was received by host. Based on the response, host was adjusting the timing step by step and recording the pass range. Through this flow host could adjust the appropriate timing settings to avoid unexpected handshaking issue.

7.2.5. Exception Handling Process

No doubt that sometimes we would face all error handling above could not recover it successfully, and we could react based on the situation.

- If there was error in response, we could re-initialize the card.
- If it was signal issue, we could set up signal status by reading data and tuning command.

7.3. Common Error Handling in SPI and SD mode

7.3.1. Time-out

Run the Retry Process. No response from CMD, it might be signal or status got problem. To avoid the infinite loop, implement a retry counter in the host so that, if the retry counter expires, the exception handling starts in the host.

7.3.2. Error Detect (CMD CRC Error)

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive response stably. Suggestion is use tuning write command to fix timing and then retry it.

7.3.3. Error Detect (Other Error) in SPI and SD mode

Run the Recovery Process.

7.3.4. Others

Most errors could be recovered by running the Recovery Process, let card come into Transfer State and then executing the flow we planned. If it does not work, please use exception method to come back initial state.

7.4. Data Error Handling in SPI and SD mode

7.4.1. Time-out

Run the Recovery Process. While the state was recovered, run the flow again.

7.4.2. Read CRC16 Error

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive data stably. Suggestion is use tuning read date to fix timing and then retry it.

7.4.3. Write CRC Status Error

Run the Recovery Process. If it got second time failure with CRC, the setting might be too margin to receive CRC status stably. Suggestion is use tuning read date to fix timing and then retry it.

7.4.4. Others

Most errors could be recovered by running the Recovery Process, let card come into Transfer State and then executing the flow we planned.

7.5. Multiple Block Write (CMD25) Process

- If Response is ADDRESS_OUT_OF_RANGE, please confirm writing address.
- If Response is DEVICE_IS_LOCKED, please stop writing data.
- If Response is COM_CRC_ERROR, run retry or tuning.

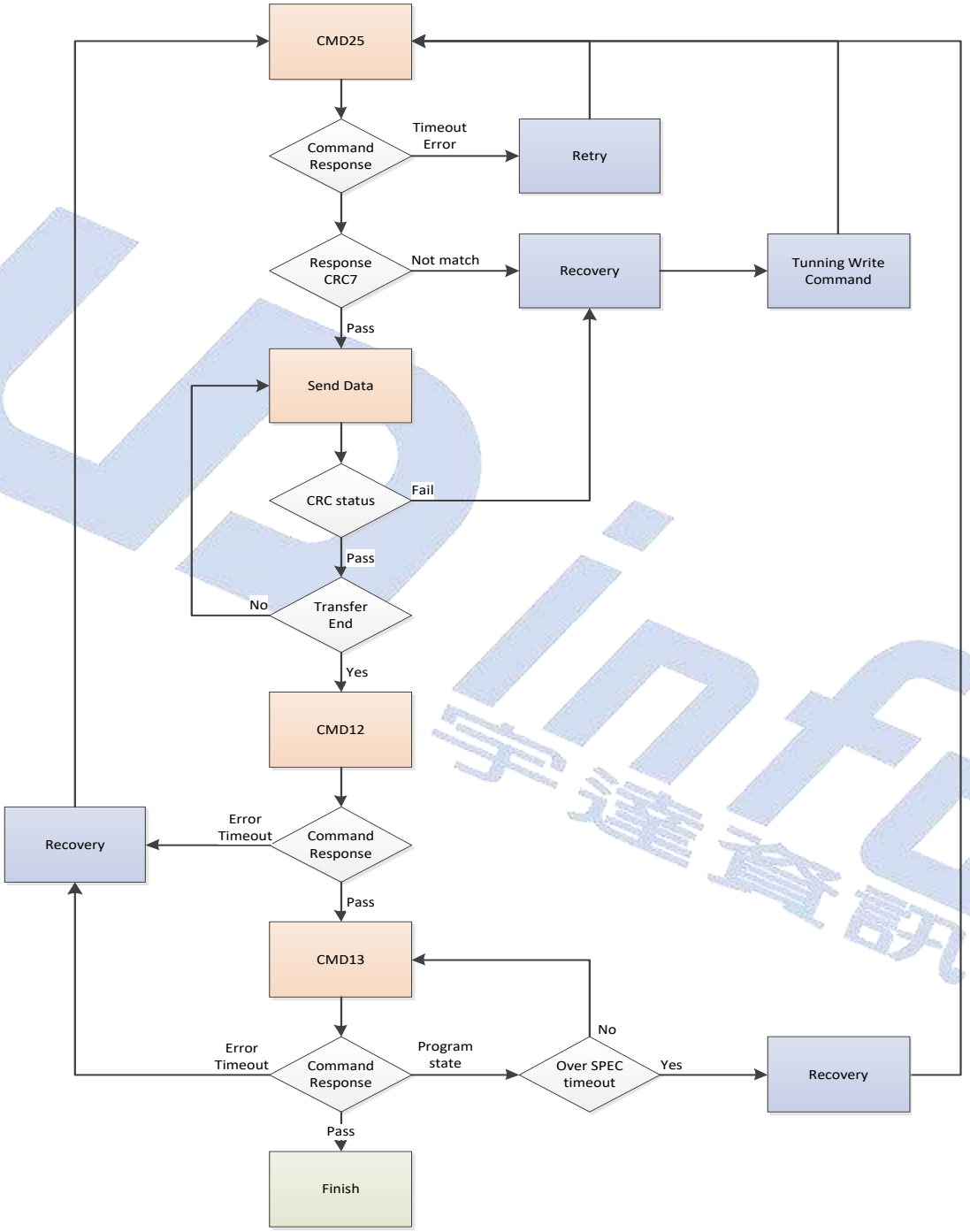


Figure 7-2 Multiple Write (CMD25) Error Handling

7.6. Retry Error handling

In order to avoid signal issue caused unexpected response from device, we could use Retry Process to fix it.

- Please make sure card state is in transfer state before issuing following commands.
- To avoid the infinite loop, implement a retry counter in the host.
- If the device could not respond to CMD13 normally, please run exception handling to recover card status.

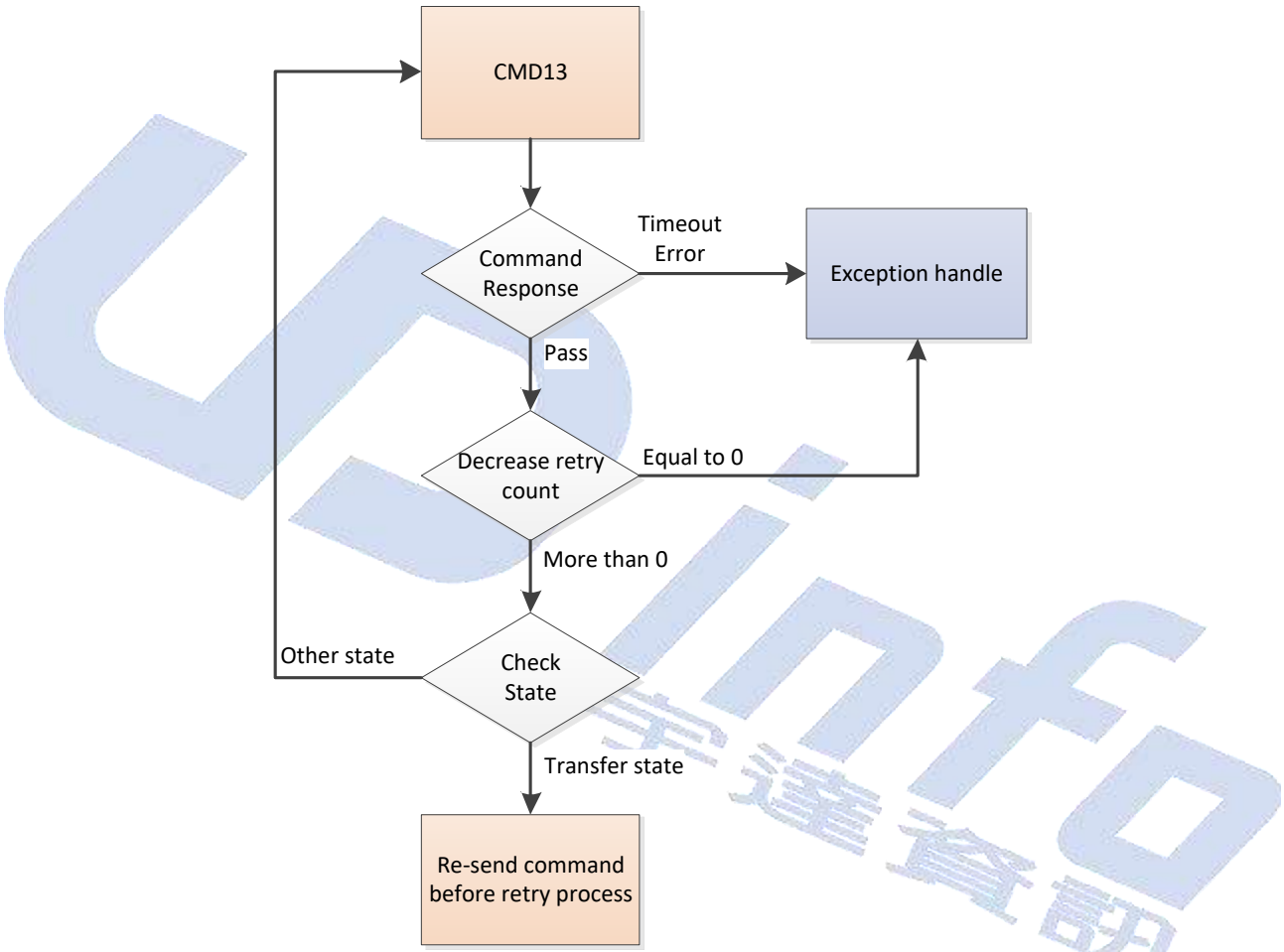


Figure 7-3 Retry Error Handling Process

7.7. Recovery Error Handling

Sometimes the device failure could not be recovered by Retry Process, it suggests to execute STOP Command (CMD12) to stop whole commands and response and then run following flow.

- Please confirm card status is in Transfer state.
- In order to avoid infinite loops, host has to set up a retry counter number.

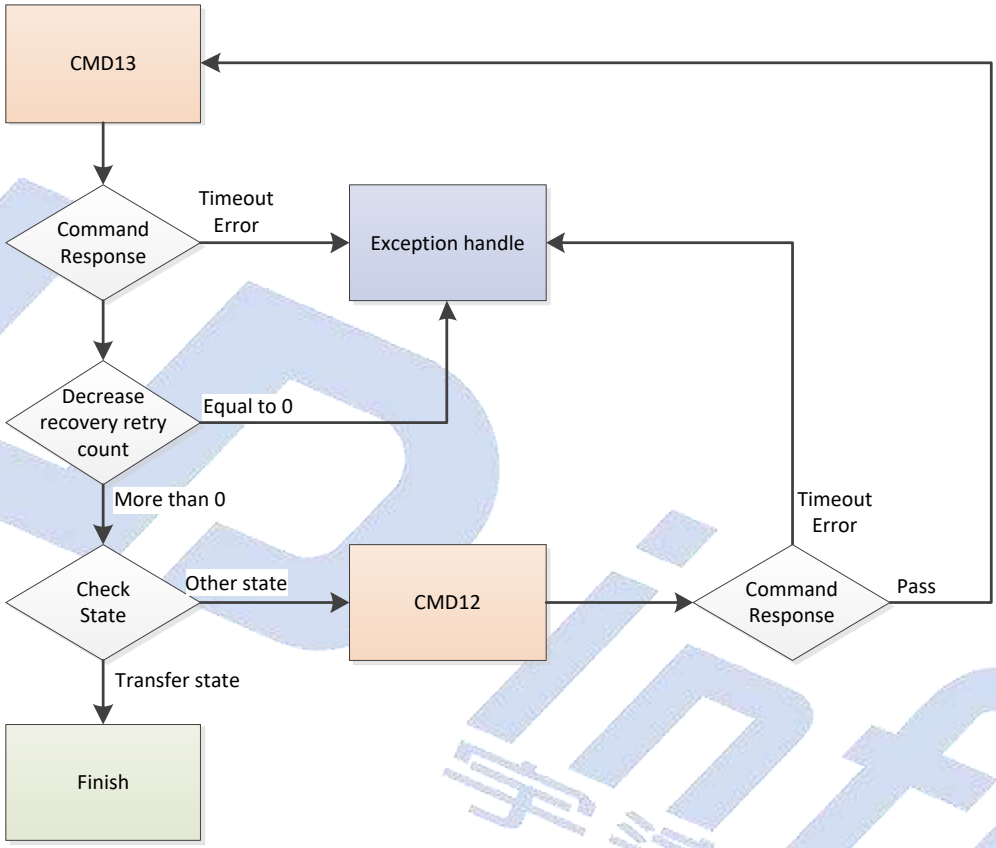


Figure 7-4 Recovery Error Handling Process

7.8. Tuning Write Command Error Handling

Reconfirm the card's pass range, to make sure card could receive host commands.

- If there was no any pass window, it might be connection issue or signal issue.
- Pass Range depends on frequency level, higher frequency makes fewer pass range.

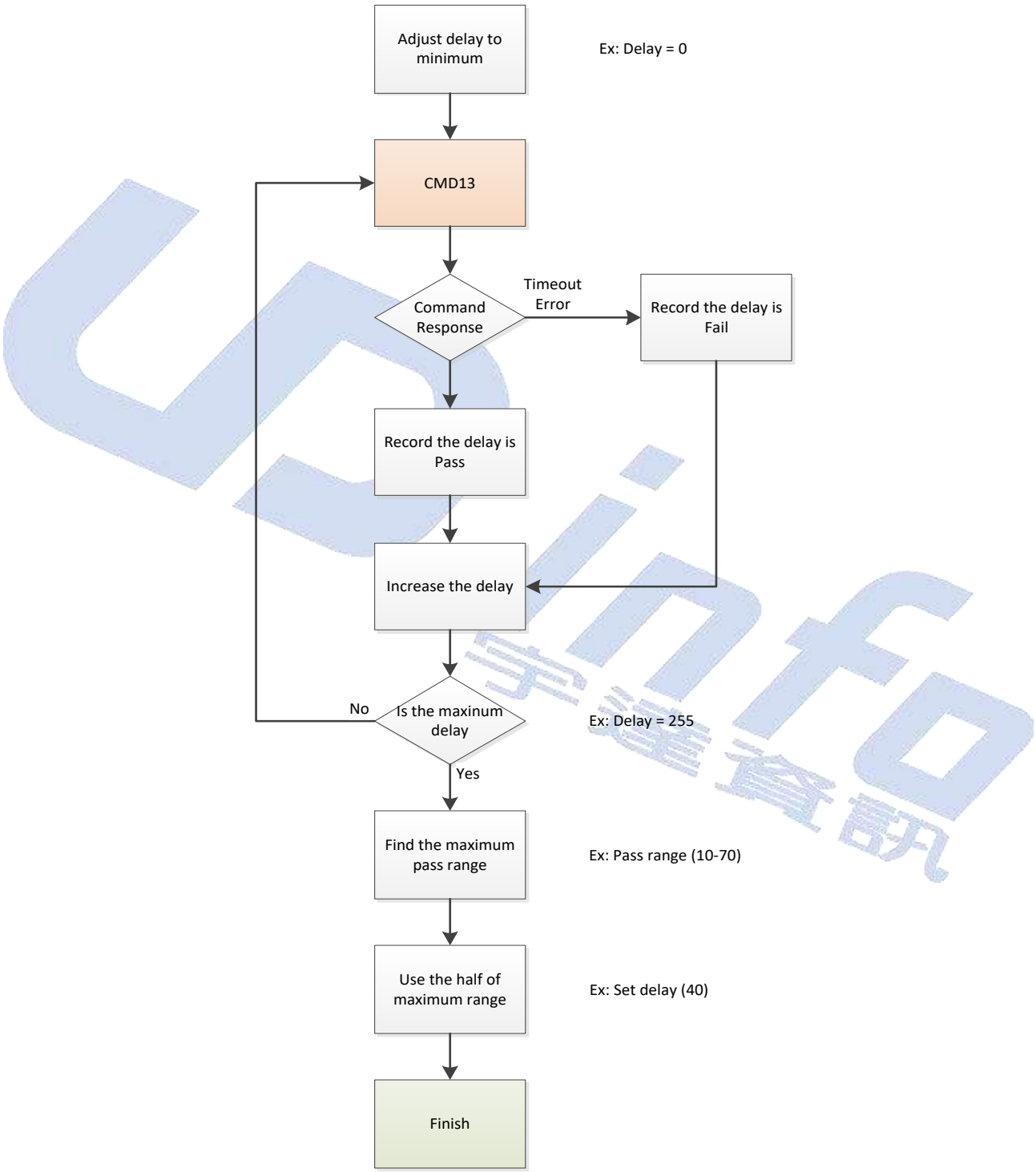


Figure 7-5 Tuning Write Command Error Handling Process

7.9. Exception Error Handling

- Error in Card's response or data output time-out, it could re-initialize the card.
- If there was CMD CRC7 issue, it could use tuning write command process to find out appropriate timing.
- If there was DAT CRC16 issue, it could use tuning read command process to find out appropriate timing.

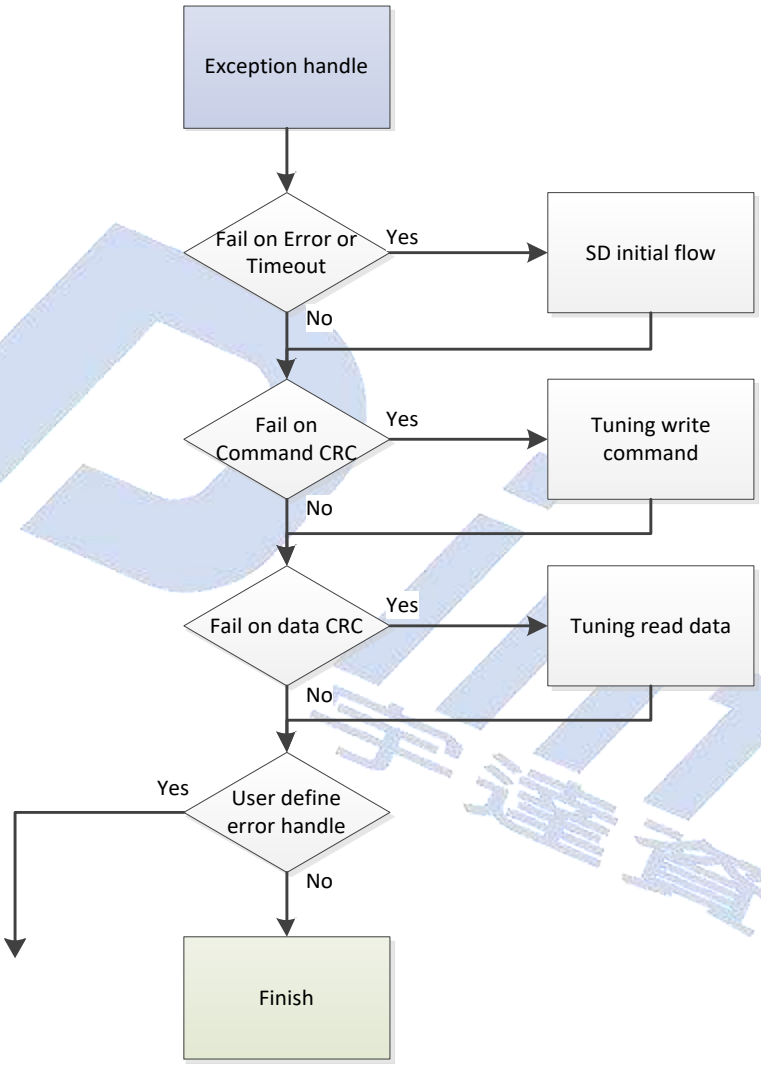


Figure 7-6 Exception Error Handling Process

7.10. Multiple Blocks Read (CMD18) Error Handling Process

- If card responded ADDRESS_OUT_OF_Range, please check writing address.
- If card responded DEVICE_IS_LOCKED, please stop writing data.
- If card responded COM_CRC_ERROR, run Retry or Tuning Process.

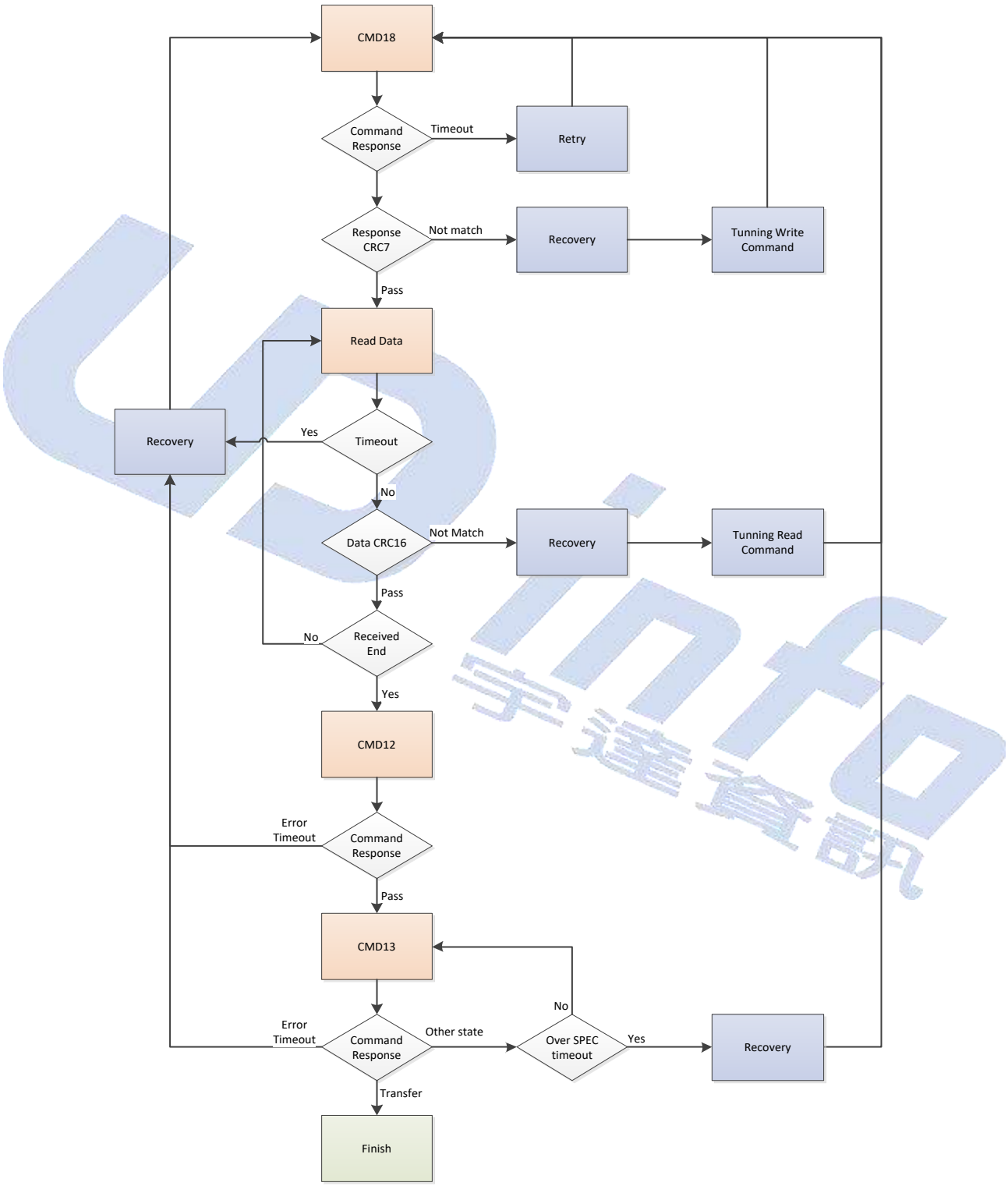


Figure 7-7 Multiple Blocks Read (CMD18) Error Handling Process

7.11. Tuning Read Data Error Handling

Reconfirm the card's pass range, to make sure host could receive card's Response and Data.

- If there was no any pass window, it might be connection issue or signal issue.
- Pass Range depends on frequency level, higher frequency makes fewer pass range.

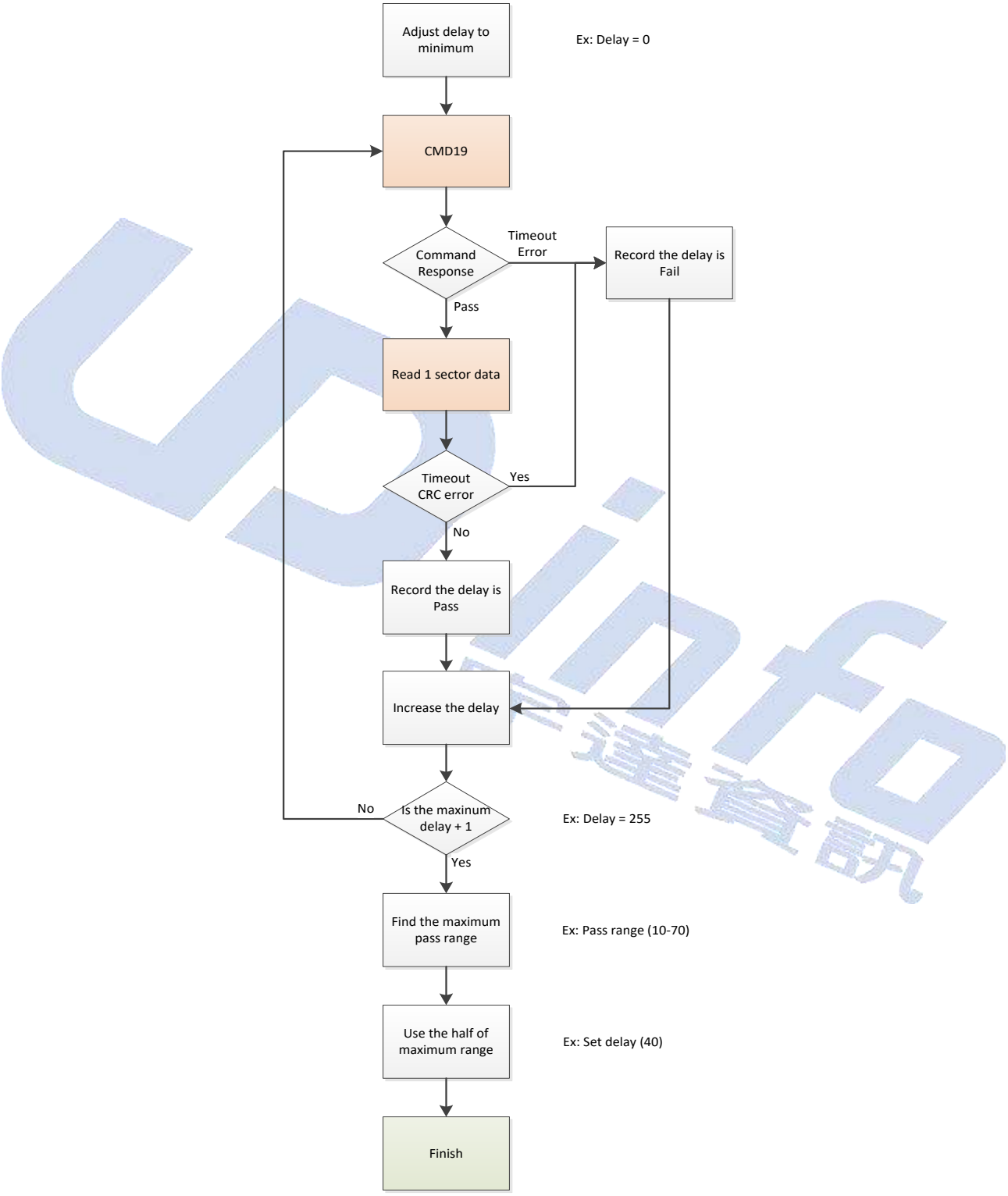


Figure 7-8 Tuning Read Data Error Handling Process

8. REGISTERS

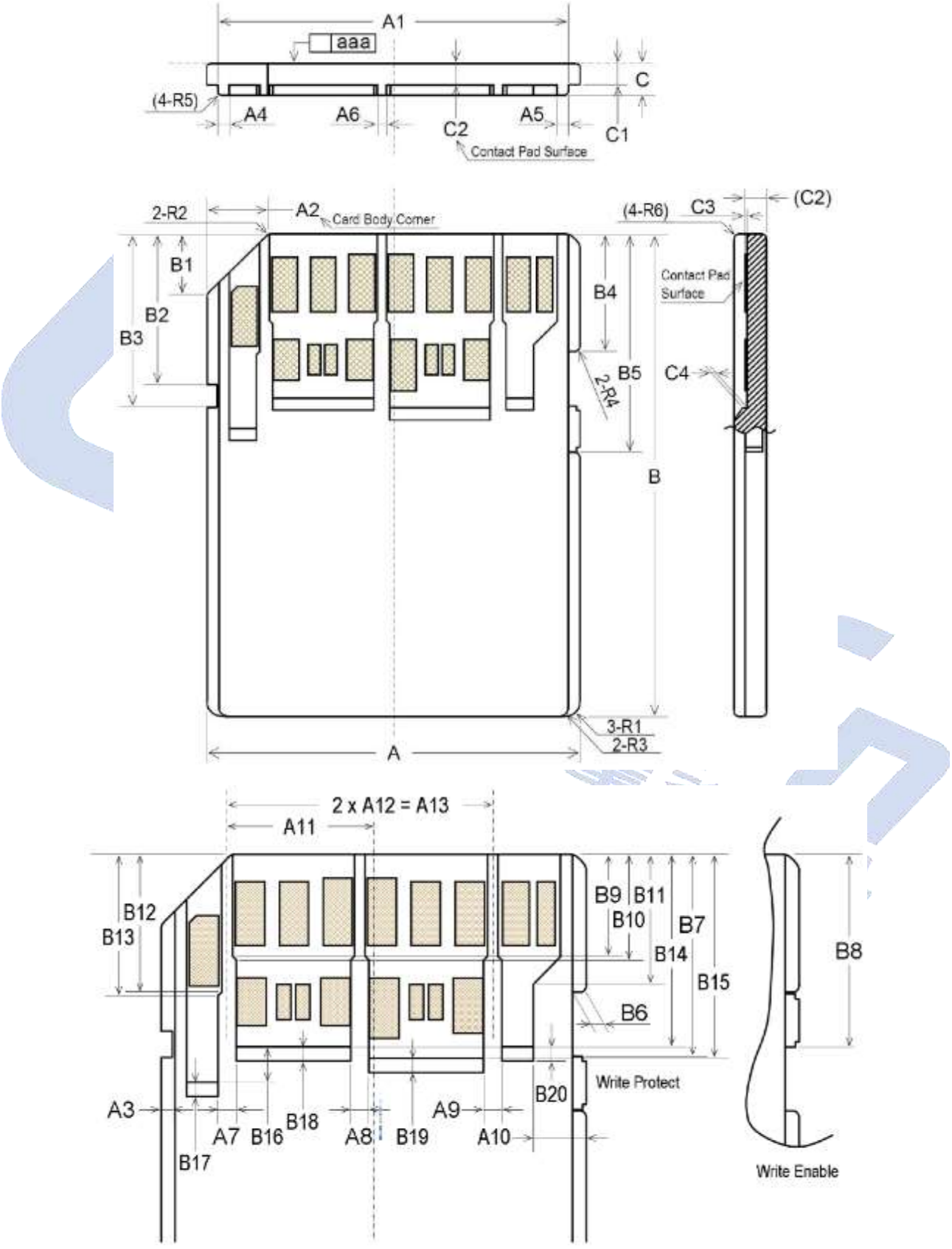
8.1. Card Registers

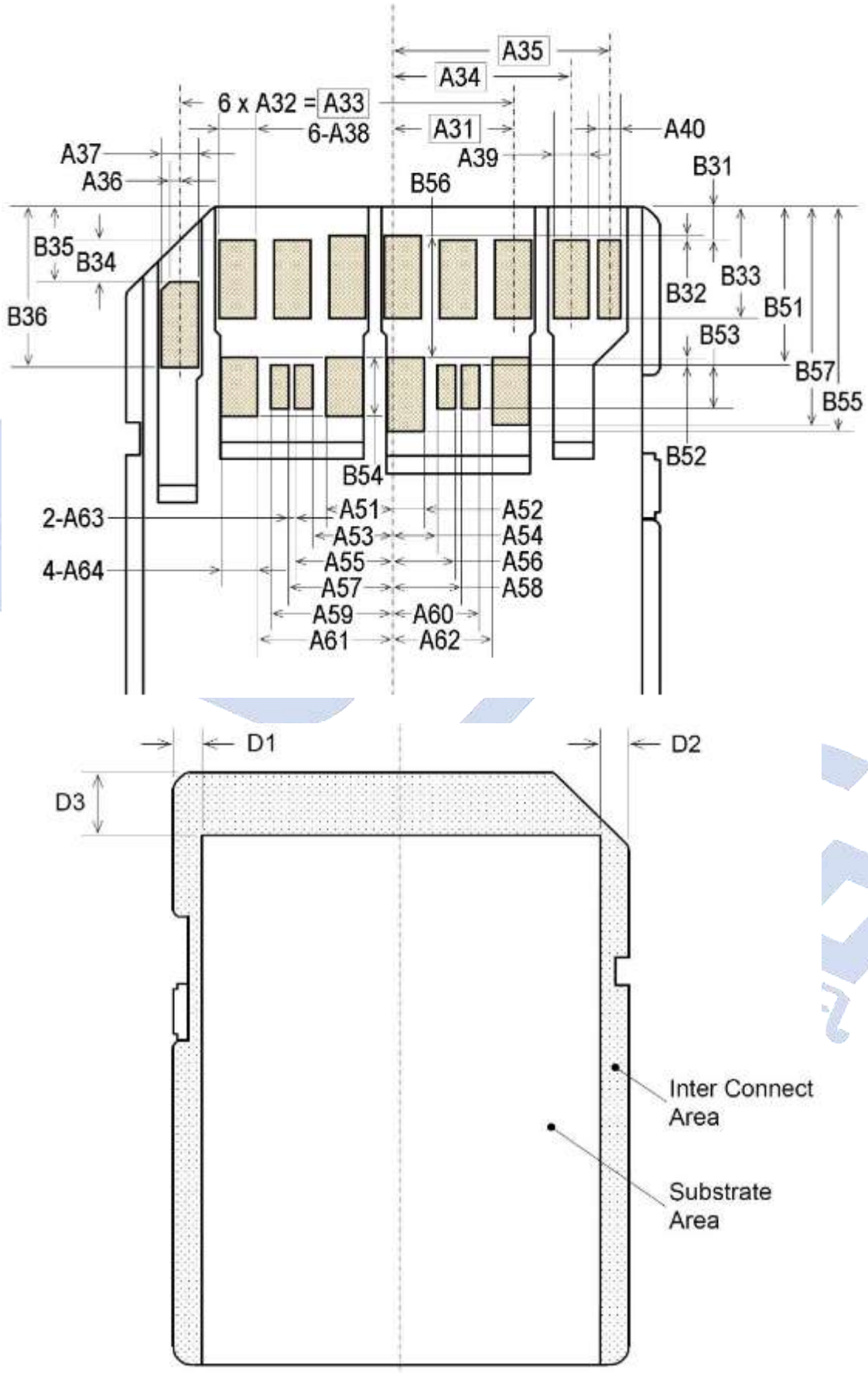
Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. **Mandatory**
RCA[1]	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. **Mandatory**
DSR	16bit	Driver Stage Register; to configure the card's output drivers. **Optional**
CSD	128bit	Card Specific Data; information about the card operation conditions. **Mandatory**
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities. **Mandatory**
OCR	32bit	Operation conditions register. **Mandatory.**
SSR	512bit	SD Status; information about the card proprietary features **Mandatory**
OCR	32bit	Card Status; information about the card status **Mandatory**

(1) RCA register is not used (or available) in SPI mode.

9. PHYSICAL DIMENSION

Dimension: 32mm(L) x 24mm(W) x 2.1mm(H)




A35
A34
6 x A32 = A33
6-A38
A31
A40
A37
A36
A39
B31
B56
B35
B34
B36
B32
B33
B51
B53
B57
B55
B52
B54
2-A63
A51
A52
A53
A54
4-A64
A55
A56
A57
A58
A59
A60
A61
A62
D1
D2
D3
Inter Connect Area
Substrate Area

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	23.9	24.0	24.1	
A1	22.4	22.5	22.5	
A2	3.85	4.00	4.15	
A3	0.60	0.75	0.90	
A4	0.55	0.70	0.85	
A5	0.55	0.70	0.85	
A6	0.45	0.60	0.75	
A7	0.90	1.05	1.20	
A8	0.90	1.05	1.20	
A9	0.90	1.05	1.20	
A10	2.85	3.00	3.15	
A11	7.975	8.125	8.275	
A12	-	7.50	-	
A13	14.85	15.00	15.15	
A31	-	5.625	-	BASIC
A32	-	2.5	-	
A33	-	15.00	-	BASIC
A34	-	8.05	-	BASIC
A35	-	9.75	-	BASIC
A36	0.25	-	-	
A37	1.40	-	-	
A38	1.40	-	-	
A39	1.10	-	-	
A40	0.90	-	-	
A51	2.675	2.825	2.975	
A52	1.425	1.575	1.725	
A53	3.325	3.475	3.625	
A54	2.075	2.225	2.375	
A55	4.125	4.275	4.425	
A56	2.875	3.025	3.175	
A57	4.325	4.475	4.625	
A58	3.075	3.225	3.375	
A59	5.125	5.275	5.425	
A60	3.875	4.025	4.175	
A61	5.775	5.925	6.075	
A62	4.525	4.675	4.825	
A63	0.20	-	-	*8
A64	1.65	-	1.85	

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
B	31.90	32.00	32.10	
B1	3.85	4.00	4.15	
B2	9.85	10.00	10.15	
B3	11.35	11.50	11.65	
B4	7.65	7.80	7.95	
B5	14.35	14.50	14.65	
B6	0.60	0.75	0.90	
B7	11.30	11.45	11.60	
B8	10.70	10.85	11.00	
B9	5.65	5.80	5.95	
B10	5.875	-	-	
B11	7.20	7.35	7.50	
B12	7.65	7.80	7.95	
B13	7.875	-	-	
B14	10.75	10.90	11.05	
B15	11.40	11.55	11.70	
B16	1.85	2.00	2.15	
B17	0.65	0.80	0.95	
B18	0.65	0.80	0.95	
B19	0.65	0.80	0.95	
B20	0.65	0.80	0.95	
B31	-	-	1.60	
B32	0.20	-	-	
B33	5.00	5.15	5.30	
B34	2.20	2.30	2.40	
B35	-	-	4.00	
B36	7.00	7.15	7.30	
B51	7.20	7.35	7.50	
B52	0.275	0.35	0.425	
B53	1.925	2.00	2.075	
B54	2.625	2.70	2.775	
B55	10.25	10.40	10.55	
B56	5.65	-	-	*8
B57	9.55	10.40	10.55	
C	1.95	2.10	2.25	
C1	1.25	1.40	1.55	
C2	1.30	1.40	1.60	
C3	0.00	-	-	
C4	-	-	0.30	

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
R1	0.90	1.00	1.10	
R2	0.40	0.50	0.60	
R3	0.35	0.50	0.65	
R4	0.15	0.3	0.45	
R5	0.15	0.3	0.45	
R6	0.15	0.3	0.45	
D1	1.50	-	-	
D2	1.50	-	-	
D3	3.4	-	-	
aaa	-	-	0.20	

1. Dimensions are in millimeters.
2. VDD2 pad must not be connected with the contact pins for xD of a combo connector.
3. Whichever of VDD1 and VDD2 may be connected first.
4. However, the legacy signal pins should be connected after VDD1.
5. The UHS-II signal pins should be connected after VDD2.
6. When a card is pushed in front of the lock position, the signal and GND contact pins are allowed to disconnect once.
7. Also refer to detailed description of Standard Size SD Card Mechanical Specification Version 3.00 for the legacy shape portion.
8. This is a double dimension. It shall satisfy this rule, after satisfying other rules.

10. PARTNUMBER DECODER

SDC-17UH$X^8X^9X^{10}X^{11}X^{12}X^{13}X^{14}X^{15}$

$X^1X^2X^3$	X^4X^5	X^6X^7	X^8 X^9 X^{10} X^{11} X^{12}	X^{13}	X^{14}	X^{15}
SDC	17	UH	032GB 064GB 128GB 256GB 512GB 001TB	A: 3D TLC Standard (-25ºC ~ +85ºC) J: 3D TLC Gold (-25ºC ~ +85ºC) V: 3D pSLC Standard (-25ºC ~ +85ºC) G: 3D pSLC Gold (-25ºC ~ +85ºC)	as below	P

X^{14} :

A: Speed Class 10 (CL10)
B: Video Speed 6 (V6)
C: Video Speed 10 (V10)
D: Video Speed 30 (V30)
U: UHS-II Class1(UHS-II, U1)
V: UHS-II Class3(UHS-II, U3)
G: App Class1 (A1)
H: App Class2 (A2)